

**SA3086**

**80ch SEGMENT /COMMON DRIVER FOR DOT MATRIX LCD**

**Technical Specification**

**Hong Kong Office**

**Room C, 19/F, Ritz plaza,  
122 Austin Road, Tsim Sha Tsui,  
Kowloon, Hong Kong**

**Tel: (852) 2622 2055  
Fax: (852) 2622 2117**

**China Tel: (86) 755 – 6117 8231**

**Web site: <http://www.redwood.hk/>**

## Introduction

The SA3086 is an LCD driver LSI that is fabricated by low power CMOS high voltage process technology. Since this product can be used as segment or common driver, for LCD panel can be configured only with this product. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

## Feature

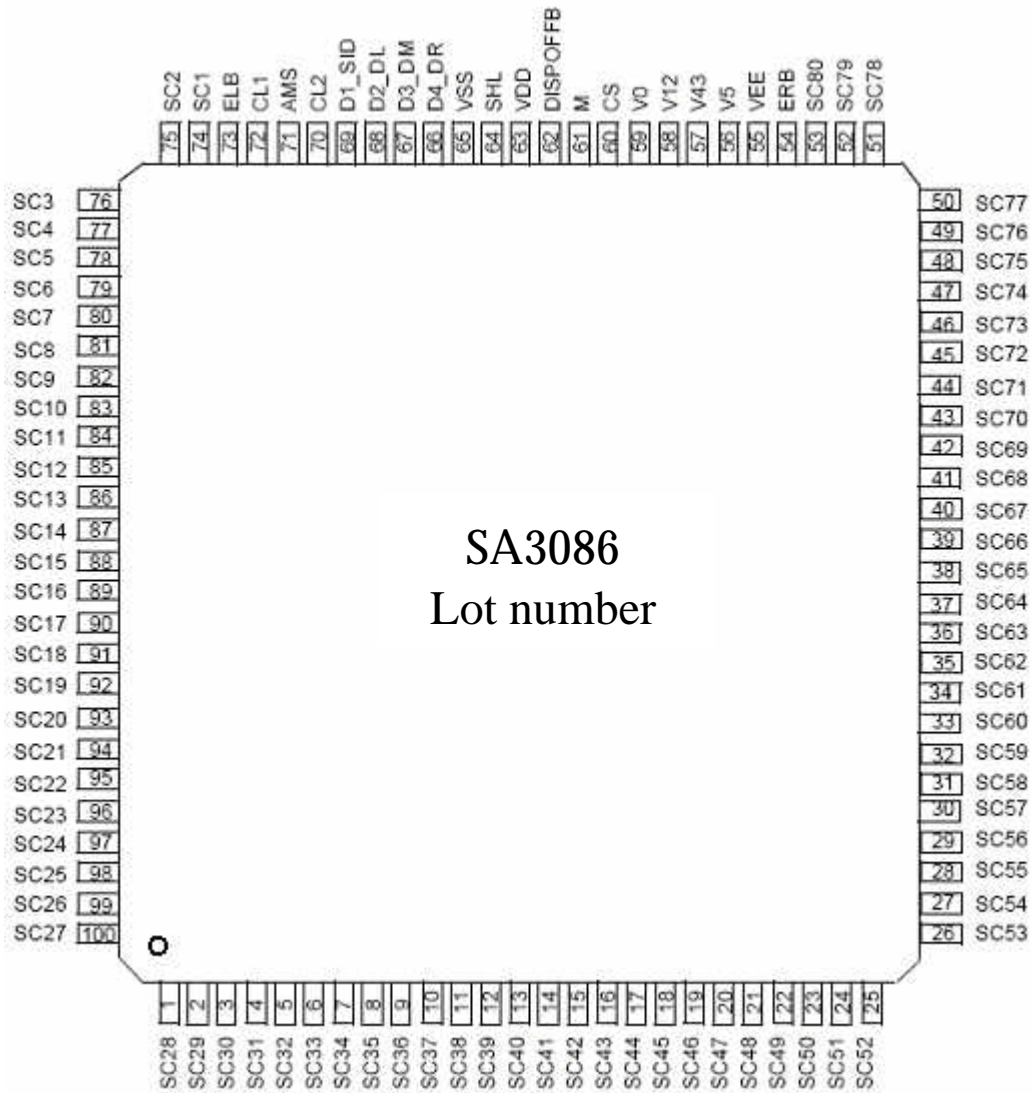
Power supply voltage	: 2.7 to 5.5V
LCD display voltage	: 6 to 28V (VDD-V <sub>EE</sub> )
Segment mode	: 4 bit parallel / 1 bit serial
Common mode	: Single or dual mode operation
Display off function	: Power down function (in segment mode)
Display Duty	: Up to 1/240

DRIVERS	
COM (cascade)	SEG (cascade)
SA3086	SA3086

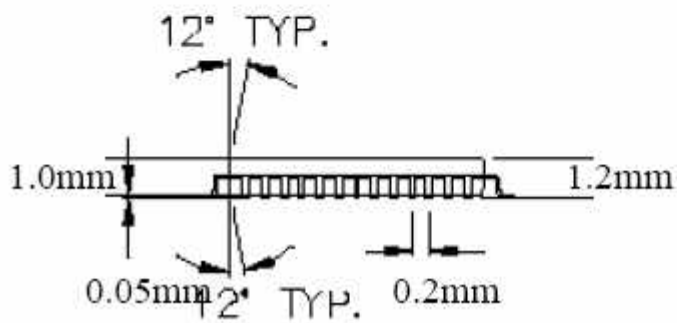
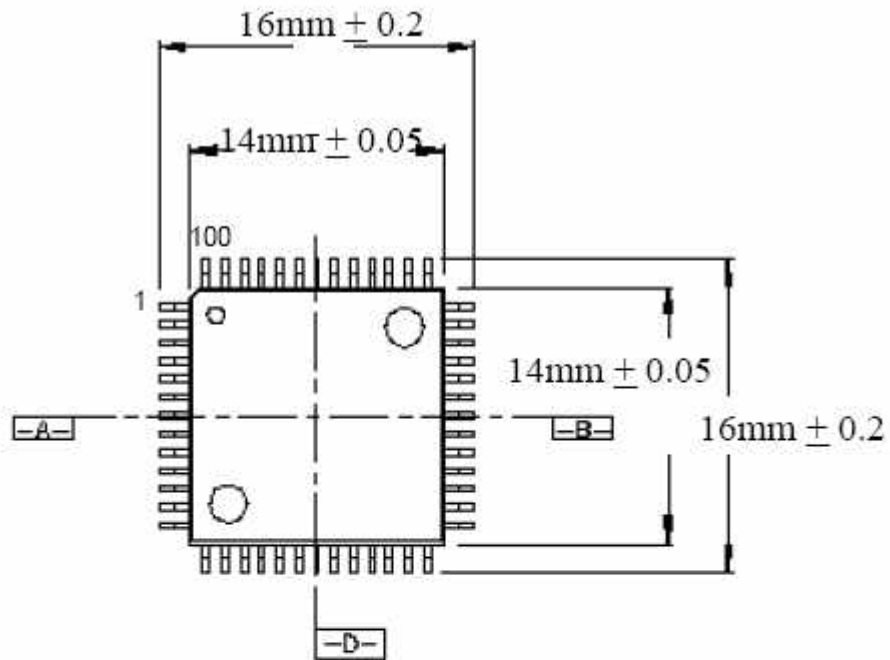
- High voltage CMOS process
- Bare die, TQFP, LQFP

## Package Information

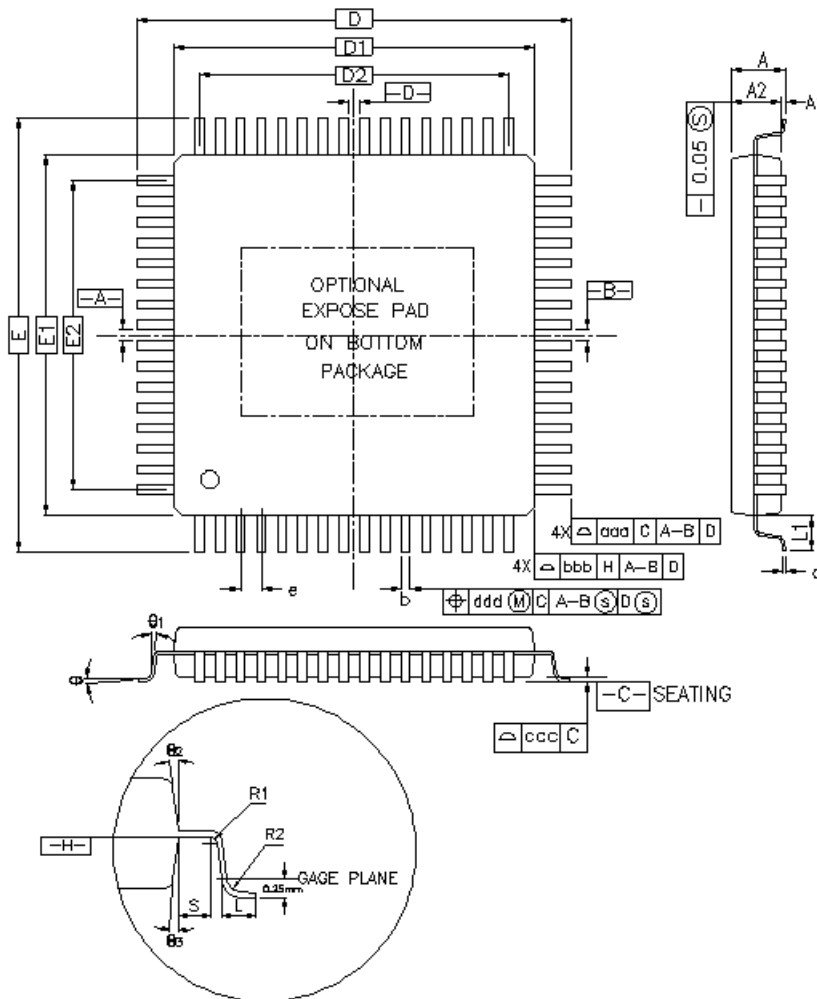
### 100 LEAD TQFP, LQFP



## TQFP Package



## LQFP Package



**Note:**  
**Option:**  
 SQUARE DOTTED LINE IS  
 E-PAD OUTLINE SIZE  
 DEPENDENT ON DIE  
 ATTACH PAD

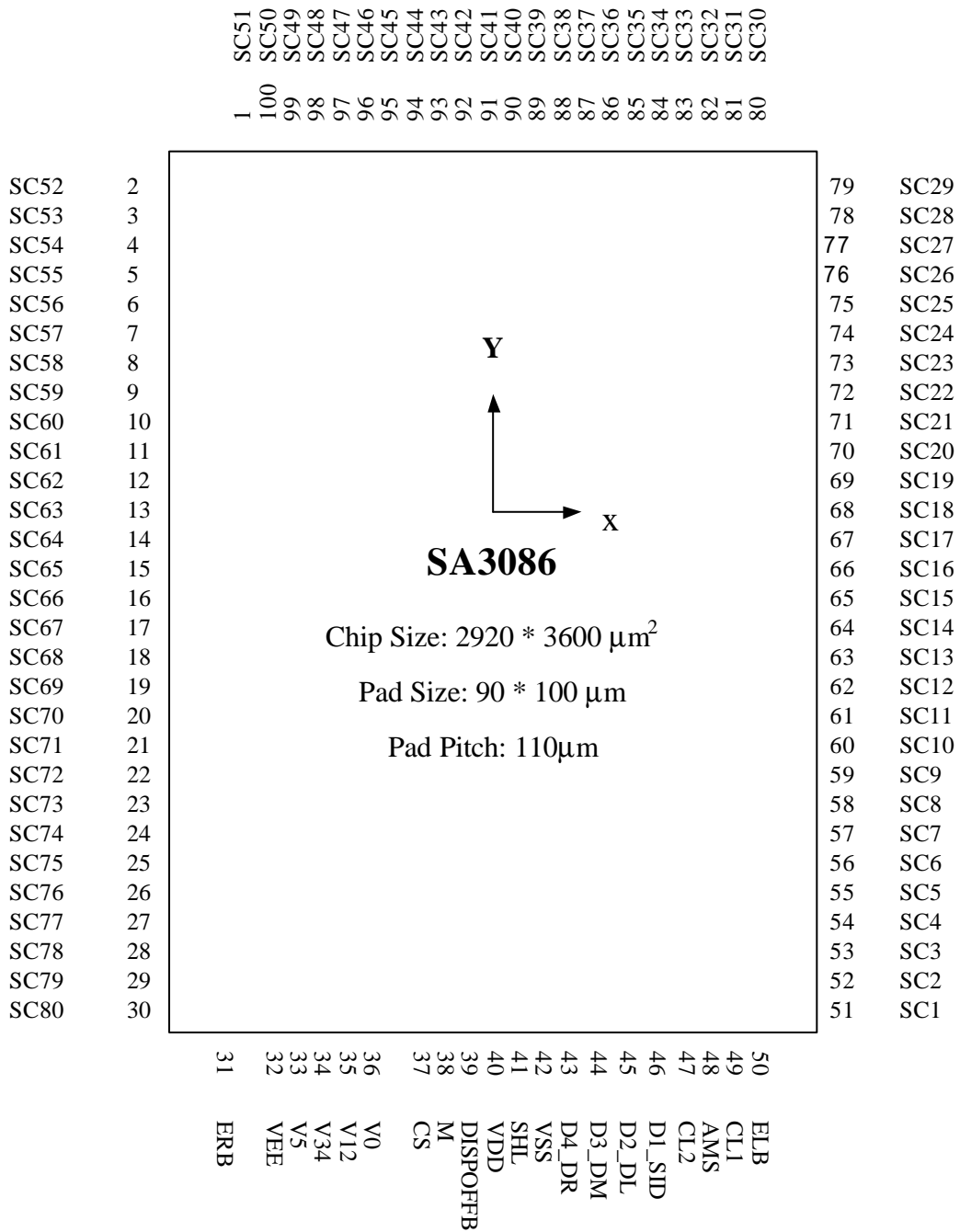
ALL DIMENSION IN MM

Symbol	Millimeter			Inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.6D	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
D2	12.00			0.472		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
E2	12.00			0.472		
R2	0.08	-	0.20	0.003	-	0.008
R1	0.06	-	-	0.003	-	-
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.004	-	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
	0.20	-	-	0.008	-	-

**Notes:**

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.

## Pad Diagram



**Die substrate should be connected to V<sub>DD</sub>.**

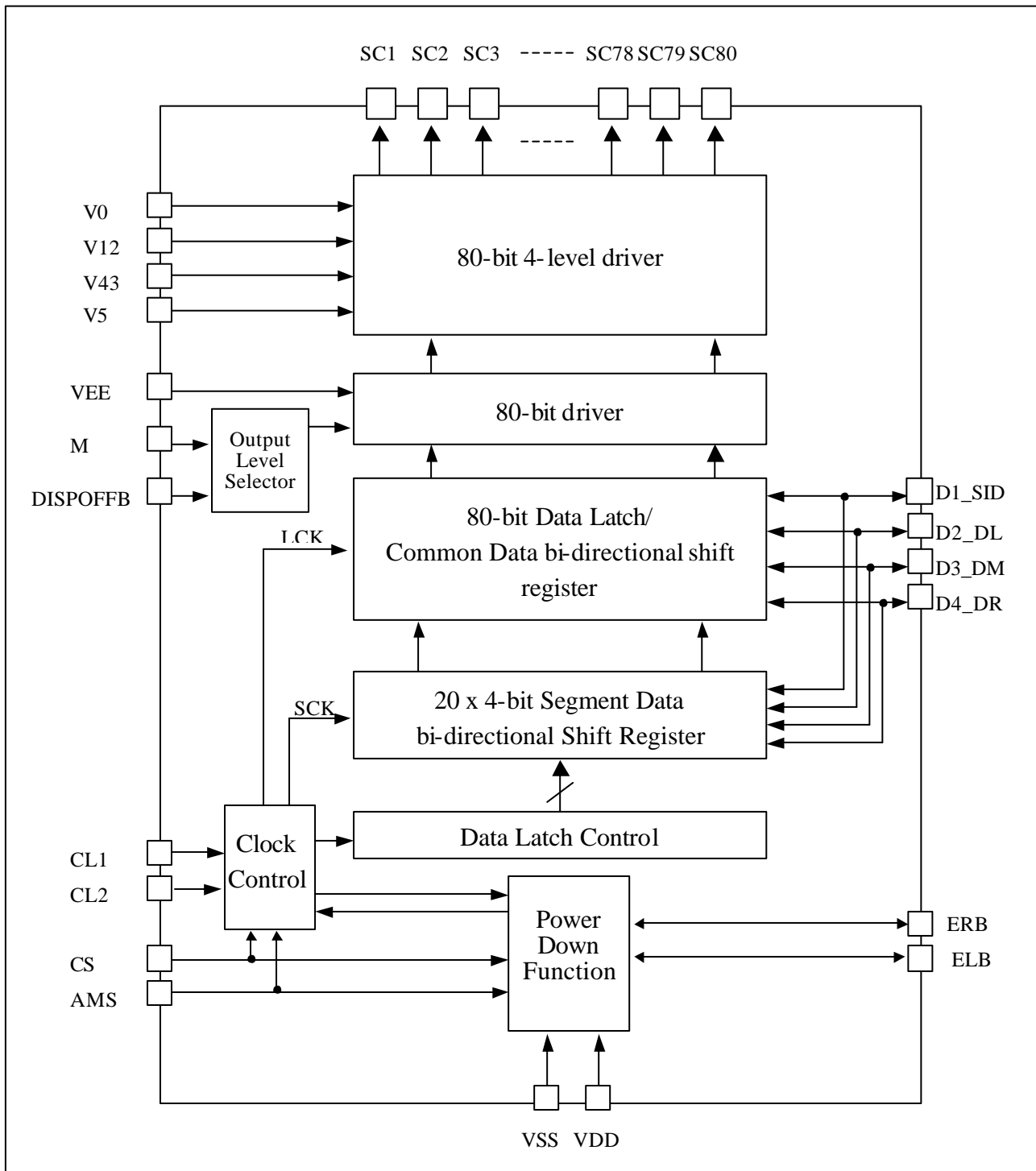
## Pad Location

No.	Name	X	Y
1	SC51	-1155.00	1684.00
2	SC52	-1344.00	1540.00
3	SC53	-1344.00	1430.00
4	SC54	-1344.00	1320.00
5	SC55	-1344.00	1210.00
6	SC56	-1344.00	1100.00
7	SC57	-1344.00	990.00
8	SC58	-1344.00	880.00
9	SC59	-1344.00	770.00
10	SC60	-1344.00	660.00
11	SC61	-1344.00	550.00
12	SC62	-1344.00	440.00
13	SC63	-1344.00	330.00
14	SC64	-1344.00	220.00
15	SC65	-1344.00	110.00
16	SC66	-1344.00	0.00
17	SC67	-1344.00	-110.00
18	SC68	-1344.00	-220.00
19	SC69	-1344.00	-330.00
20	SC70	-1344.00	-440.00
21	SC71	-1344.00	-550.00
22	SC72	-1344.00	-660.00
23	SC73	-1344.00	-770.00
24	SC74	-1344.00	-880.00
25	SC75	-1344.00	-990.00
26	SC76	-1344.00	-1100.00
27	SC77	-1344.00	-1210.00
28	SC78	-1344.00	-1320.00
29	SC79	-1344.00	-1430.00
30	SC80	-1344.00	-1540.00
31	ERB	-1090.00	-1684.00
32	VEE	-934.40	-1684.00
33	V5	-824.40	-1684.00
34	V43	-714.40	-1684.00

No.	Name	X	Y
35	V12	-604.40	-1684.00
36	V0	-494.40	-1684.00
37	CS	-334.70	-1684.00
38	M	-224.70	-1684.00
39	DISPOFFB	-114.70	-1684.00
40	VDD	-4.70	-1684.00
41	SHL	105.30	-1684.00
42	VSS	215.30	-1684.00
43	D4_DR	325.30	-1684.00
44	D3_DM	435.30	-1684.00
45	D2_DL	545.30	-1684.00
46	D1_SID	655.30	-1684.00
47	CL2	765.30	-1684.00
48	AMS	875.30	-1684.00
49	CL1	985.30	-1684.00
50	ELB	1095.30	-1684.00
51	SC1	1344.00	-1540.00
52	SC2	1344.00	-1430.00
53	SC3	1344.00	-1320.00
54	SC4	1344.00	-1210.00
55	SC5	1344.00	-1100.00
56	SC6	1344.00	-990.00
57	SC7	1344.00	-880.00
58	SC8	1344.00	-770.00
59	SC9	1344.00	-660.00
60	SC10	1344.00	-550.00
61	SC11	1344.00	-440.00
62	SC12	1344.00	-330.00
63	SC13	1344.00	-220.00
64	SC14	1344.00	-110.00
65	SC15	1344.00	0.00
66	SC16	1344.00	110.00
67	SC17	1344.00	220.00
68	SC18	1344.00	330.00

No.	Name	X	Y
69	SC19	1344.00	440.00
70	SC20	1344.00	550.00
71	SC21	1344.00	660.00
72	SC22	1344.00	770.00
73	SC23	1344.00	880.00
74	SC24	1344.00	990.00
75	SC25	1344.00	1100.00
76	SC26	1344.00	1210.00
77	SC27	1344.00	1320.00
78	SC28	1344.00	1430.00
79	SC29	1344.00	1540.00
80	SC30	1155.00	1684.00
81	SC31	1045.00	1684.00
82	SC32	935.00	1684.00
83	SC33	825.00	1684.00
84	SC34	715.00	1684.00
85	SC35	605.00	1684.00
86	SC36	495.00	1684.00
87	SC37	385.00	1684.00
88	SC38	275.00	1684.00
89	SC39	165.00	1684.00
90	SC40	55.00	1684.00
91	SC41	-55.00	1684.00
92	SC42	-165.00	1684.00
93	SC43	-275.00	1684.00
94	SC44	-385.00	1684.00
95	SC45	-495.00	1684.00
96	SC46	-605.00	1684.00
97	SC47	-715.00	1684.00
98	SC48	-825.00	1684.00
99	SC49	-935.00	1684.00
100	SC50	-1045.00	1684.00

Block Diagram





## Block Description

Name	Function	COM/SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control timing according to the input of CL1, CL2 and control inputs (CS, AMS). In common driver application, this block generates shift clock (LCK) for the common data bidirectional shift register.	COM/SEG
Data latch control	Determines the direction of segment data shift, and input data of each bidirectional shift register. In case of 4-bit segment data parallel transfer mode, 4-bit unit shifts data. In case of common driver application mode, data is transferred to the common data shift register directly, so this block is not work.	SEG
Power down function	Controls the clocks enable state of current driver according to the input value of enable pin (ELB or ERB). If enable input value is 'Low', every clock of the current driver is enabled and the clock control block works. But if enable input is 'High', current driver is disabled and the input data value has no effect to the output level. So power consumption can be lowered.	SEG
Output level selector	Control the output voltage level according to the input control pin (M and DISPOFFB) (refer to Pin Description).	COM/SEG
80-bit data latch / common data bidirectional shift register	In segment driver application, the data from the 20x4-bit segment data shift register are latched for segment driver output. When single-type common driver application, 1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. When dual-type common application mode, 80-bit two divides registers blocks and controlled independently (refer to NOTE 3).	COM/SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are logical voltage level and the outputs of this block are high voltage level value. And this value is input to the driver.	COM/SEG
80-bit 4-level driver	Selects the output voltage level according to the M and latched data value. If the data value is 'High' the driver output is selected voltage level (V0 or V5), and in the reverse case the driver output value is non-selected level (V12 or V43). In segment driver application, non-selected output value is V2 or V3. And when common driver application, this value becomes V1 or V4.	COM/SEG

## Pin Description

Pin (No)	Input/Output	Name	Description	Interface																		
VDD (40)	Power	Operating Voltage	Logic power supply (2.7 to 5.5V)	Power																		
VSS (42)			0V (GND)																			
VEE (32)		Driver Supply Voltage	Power supply for driving the LCD																			
V0, V12, V43, V5 (33-36)	Input	LCD driver output voltage level	Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source (refer to NOTE 2).	Power																		
SC1 ~ SC80 (1-30, 51-100)	Output	LCD driver output	Display data output pin, which corresponds to the respective latch contents. One of V0, V12, V43 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to NOTE 1).	LCD																		
CL1 (49)	Input	Data latch clock	<ul style="list-style-type: none"> <li>In segment application, CL1 is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse 'High' level initializes power-down function block.</li> <li>In common driver application, CL1 is used as shifting clock of common output data.</li> </ul>	Controller																		
CL2 (47)	Input	Data shift clock	Clock pulse input for the bidirectional shift register. <ul style="list-style-type: none"> <li>In segment application, CL2 is used as display data latch signal at the falling edge. This pulse, which was input when the enable bit (ELB/ERB) is not active condition, is invalid.</li> <li>In common application, the data is shifted to 80-bit common data bidirectional shift register by the CL1 clock. So this clock pin is not used (Open or connect this to VDD)</li> </ul>	Controller																		
M (38)	Input	Alternate signal for LCD driver output	Alternate signal input pin for LCD driving. Normal frame inversion signal is input to this pin.	Controller																		
DISPOFFB (39)	Input	Display off control	Control input pin to fix the driver output (SC1~SC80) to V0 level, during 'Low' value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.	Controller																		
CS (37)	Input	COM/SEG mode control	When CS = 'Low', SA3086 is used as 80-bit segment driver. When CS = 'High', SA3086 is set to 80-bit common driver.	VDD /Vss																		
AMS (48)	Input	Application mode select	According to the input value of the AMS and the CS pin, application mode of SA3086 is different as below. <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th>CS</th> <th>AMS</th> <th>Application mode</th> <th>COM/SEG</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>4-bit parallel interface mode</td> <td rowspan="2">SEG</td> </tr> <tr> <td>L</td> <td>H</td> <td>1-bit serial interface mode</td> </tr> <tr> <td>H</td> <td>L</td> <td>Single-type application mode</td> <td rowspan="2">COM</td> </tr> <tr> <td>H</td> <td>H</td> <td>Dual-type application mode</td> </tr> </tbody> </table>	CS	AMS	Application mode	COM/SEG	L	L	4-bit parallel interface mode	SEG	L	H	1-bit serial interface mode	H	L	Single-type application mode	COM	H	H	Dual-type application mode	VDD /Vss
CS	AMS	Application mode	COM/SEG																			
L	L	4-bit parallel interface mode	SEG																			
L	H	1-bit serial interface mode																				
H	L	Single-type application mode	COM																			
H	H	Dual-type application mode																				

## Pin Description (continued)

Pin (No)	Input/Output	Name	Function	Interface											
D1_SID, D2_DL, D3_DM, D4_DR (43-46)	Input / Output	Display data input serial input data / left, right data input / output	<ul style="list-style-type: none"> <li>In segment application, these pins are used as 4-bit data input pin (When parallel mode), or D1SID is used as serial data input pin and other pins are not used. (Open or connect this to VDD) (When serial mode).</li> <li>In common application, the data are shifted from D2DL (D4DR) to D4DR (D2DL), when single-type application mode (AMS = 'Low'). In dual-type application case, the data are shifted from D2DL and D3DM (D4DR and D3DM) to D4-DR (D2 DL). In each case the direction of data shift is determined by SHL input, (refer to NOTE 3, NOTE4)</li> </ul>	Controller											
SHL (41)	Input	Shift direction control	When SHL = 'Low', data is shifted from left to right When SHL = 'High', the direction is reversed, (refer to NOTE 3)	VDD /Vss											
ELB, ERB (50,31)	Input / Output	Enable data input / output	<ul style="list-style-type: none"> <li>In segment application, only when enable input (ELB or ERB) is 'Low', the internal operation is enabled (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. (Refer to NOTE 4)</li> </ul> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">SHL</th> <th colspan="2">SEGMENT DRIVER</th> </tr> <tr> <th>ELB</th> <th>ERB</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>Output (Last open)</td> <td>Input (First Vss)</td> </tr> <tr> <td>H</td> <td>Input (First Vss)</td> <td>Output (Last open)</td> </tr> </tbody> </table> <ul style="list-style-type: none"> <li>In common application, power down function is not used. (Open)</li> </ul>	SHL	SEGMENT DRIVER		ELB	ERB	L	Output (Last open)	Input (First Vss)	H	Input (First Vss)	Output (Last open)	-
SHL	SEGMENT DRIVER														
	ELB	ERB													
L	Output (Last open)	Input (First Vss)													
H	Input (First Vss)	Output (Last open)													

### Note1. Output level control

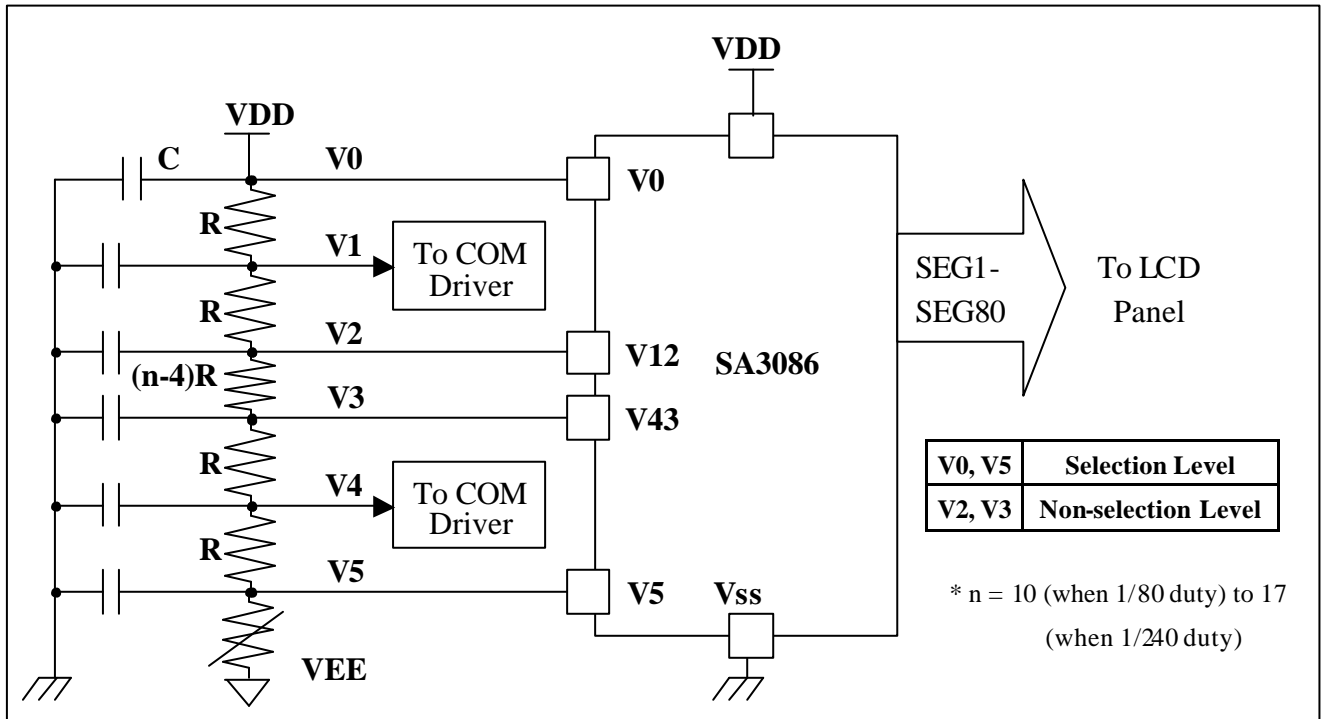
X: Don't care

M	Latched data	DISPOFFB	Output level (SC1 ~ SC80)	
			SEG Mode	COM Mode
L	L	H	V12 (V2)	V12 (V1)
L	H	H	V0	V5
H	L	H	V43 (V3)	V43 (V4)
H	H	H	V5	V0
X	X	L	V0	V0

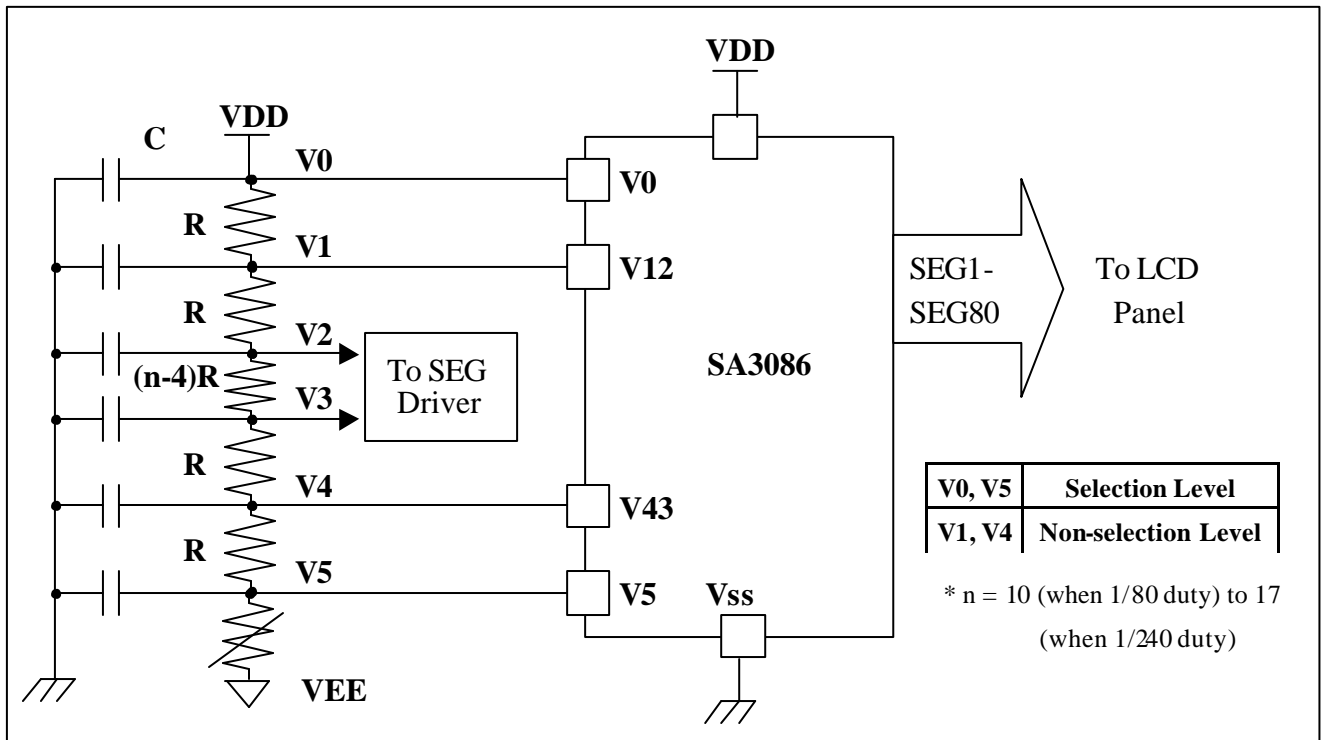
- In display off mode, the voltage of V0 is keep for the input of chip.**

## Note2. LCD Driving Voltage Application Circuit

(1) Segment driver application (CS = 'Low')



(2) Common driver application (CS = 'High')



### Note3. Data Shift Direction according to Control Signals

(1) When CS = 'Low' (segment driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	4-Bit Parallel Data Transfer Mode (SEG)		D1_SID, D2_DL, D3_DM, D4_DR
	H			
H	L	1-Bit Serial Data Transfer Mode (SEG)		D1_SID
	H			

When CS = 'High' (common driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	Single-type Application Mode (COM)		D2_DL
	H			D4_DR
H	L	Dual-type Application Mode (COM)		D2_DL, D3_DM
	H			D4_DR, D3_DM

### Note4. Usage of Data Pins

COM/SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS = 'Low')	4 bit parallel interface mode (AMS = 'Low')	X	D1 (input)	D2 (input2)	D3 (input3)	D4 (input4)
	1 bit serial interface mode (AMS = 'Low')	X	SID (input)	Connect to VDD		
COM (CS = 'High')	Single type application mode (AMS = 'Low')	L	Open	DL (input)	Open	DR (output)
		H		DL (output)		DR (input)
	Dual type application mode (AMS = 'High')	L	Open	DL (input1)	DM (input2)	DR (output2)
		H		DL (output2)	DM (input2)	DR (input1)

### Maximum Absolute Limit

Characteristic	Symbol	Value	Unit
Power supply voltage	$V_{DD}$	-0.3 - +7.0	V
Driver supply voltage	$V_{LCD}$	0 - 30	
Input voltage	$V_{IN}$	-0.3 - $V_{DD} + 0.3$	
Operating temperature	$T_{opr}$	-30 - +85	°C
Storage temperature	$T_{stg}$	-55 - +150	

\* **Note:** Voltage greater than above may do damage to the circuit.

## Electrical Characteristics

### DC Characteristics

#### (1) Segment Driver Application

(V<sub>SS</sub> = 0V, T<sub>a</sub> = -30 to +85°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Operating Voltage 1	V <sub>DD</sub>	-	2.7	-	5.5	V	
	V <sub>LCD</sub>	V <sub>IN</sub> = V <sub>DD</sub> - V <sub>EE</sub>	6	-	28		
Input voltage (1)	V <sub>IH</sub>	-	0.8V <sub>DD</sub>	-	V <sub>DD</sub>		
	V <sub>IL</sub>	-	0	-	0.2V <sub>DD</sub>		
Output voltage (2)	V <sub>OH</sub>	I <sub>OH</sub> = -0.4mA	V <sub>DD</sub> -0.4	-	-	V	
	V <sub>OL</sub>	I <sub>OL</sub> = 0.4mA	-	-	0.4		
Input leakage current 1 (1)	I <sub>IL1</sub>	V <sub>IN</sub> = V <sub>DD</sub> to V <sub>SS</sub>	-10	-	10	μA	
Input leakage current 2 (3)	I <sub>IL2</sub>	V <sub>IN</sub> = V <sub>DD</sub> to V <sub>EE</sub>	-25	-	25		
On resistance (4)	R <sub>ON</sub>	I <sub>ON</sub> = 100μA	-	2	4	kΩ	
Supply current (5)	I <sub>STBY</sub>	f <sub>CL1</sub> = 0Hz, M = V <sub>SS</sub>	V <sub>SS</sub> pin	-	-	6	μA
	I <sub>DD</sub>	f <sub>CL1</sub> = 32kHz f <sub>M</sub> = 80 Hz	V <sub>DD</sub> = 5V	-	-	5	mA
			V <sub>DD</sub> = 3V	-	-	2	
	I <sub>EE</sub>		V <sub>DD</sub> = 5V	-	-	500	μA

#### Notes:

- Applied to CL1, CL2, ELB, ERB, D1\_SID – D4\_DR, SHL, DISPOFFB, M, CS, AMS pin
- ELB, ERB pin
- V0, V12, V43, V5 pin
- V<sub>LCD</sub> = V<sub>DD</sub> - V<sub>EE</sub>, V0 = V<sub>DD</sub> = 5V, V5 = V<sub>EE</sub> = -23 V  
V12 = V<sub>DD</sub>-2/n (V<sub>LCD</sub>), V43 = V<sub>EE</sub>+2/n (V<sub>LCD</sub>), n = 17 (1/240 duty, 1/17 bias)
- V0 = V<sub>DD</sub>, V12 = 1.71V (V<sub>DD</sub> = 5V) or -0.06V (V<sub>DD</sub> = 3V),  
V43 = -19.71V (V<sub>DD</sub> = 5V) or -19.94V (V<sub>DD</sub> = 3V), V5 = V<sub>EE</sub> = -23V, no-load condition (1/240 duty, 1/17 bias)  
4-bit parallel interface mode  
I<sub>STBY</sub>: V<sub>DD</sub> = 5V, f<sub>CL2</sub> = 0Hz, SHL = V<sub>SS</sub>, DISPOFFB = V<sub>SS</sub>, M = V<sub>SS</sub>, display data pattern = 0000  
I<sub>DD</sub>: V<sub>DD</sub> = 3V, f<sub>CL2</sub> = 4MHz, display data pattern = 0101, DISPOFFB = V<sub>DD</sub>  
V<sub>DD</sub> = 5 V, f<sub>CL2</sub> = 5.12MHz, display data pattern = 0101, DISPOFFB = V<sub>DD</sub>  
I<sub>EE</sub>: V<sub>DD</sub> = 5V, f<sub>CL2</sub> = 5.12MHz, display data pattern = 0101, V<sub>EE</sub> pin, DISPOFFB = V<sub>DD</sub>



## DC Characteristic (Continued)

### (2) Common Driver Application

(V<sub>SS</sub> = 0V, T<sub>a</sub> = -30 to +85°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Operating voltage1	V <sub>DD</sub>	-	2.7	-	5.5	V	
	V <sub>LCD</sub>	V <sub>IN</sub> = V <sub>DD</sub> - V <sub>EE</sub>	6	-	28		
Input voltage (1)	V <sub>IH</sub>	-	0.8V <sub>DD</sub>	-	V <sub>DD</sub>	V	
	V <sub>IL</sub>	-	0	-	0.2V <sub>DD</sub>		
Output voltage (3)	V <sub>OH</sub>	I <sub>OH</sub> = -0.4mA	V <sub>DD</sub> -0.4	-	-	V	
	V <sub>OL</sub>	I <sub>OL</sub> = 0.4mA	-	-	0.4		
Input leakage current 1 (1)	I <sub>IL1</sub>	V <sub>IN</sub> = V <sub>DD</sub> to V <sub>SS</sub>	-10	-	10	μA	
Input leakage current 2 (2)	I <sub>IL2</sub>	V <sub>IN</sub> = 0V, V <sub>DD</sub> = 5V (Pull Up)	-50	-125	-250		
Input leakage current 3 (4)	I <sub>IL3</sub>	V <sub>IN</sub> = V <sub>DD</sub> to V <sub>SS</sub>	-25	-	25		
On resistance (5)	R <sub>ON</sub>	I <sub>ON</sub> = 100μA	-	2	4	kΩ	
Supply current (6)	I <sub>STBY</sub>	f <sub>CL1</sub> = 0Hz	V <sub>SS</sub> pin	-	-	6	μA
	I <sub>DD</sub>	f <sub>CL1</sub> = 32kHz	V <sub>DD</sub> = 5V	-	-	200	
			V <sub>DD</sub> = 3V	-	-	120	
	I <sub>EE</sub>	f <sub>M</sub> = 80 Hz	V <sub>DD</sub> = 5V	-	-	150	

#### Notes:

- Applied to CL1, D2\_DL (SHL = LOW), D4\_DR (SHL = HIGH), SHL, DISPOFFB, M, CS, AMS pin
- Pull-up input pins: CL2, D1\_SID, D3\_DM (AMS = HIGH), ELB (SHL = LOW), ERB (SHL = HIGH)
- D2\_DL (SHL = HIGH), D4\_DR (SHL = LOW) pin
- V0, V12, V43, V5 pin
- V<sub>KCD</sub> = V<sub>DD</sub> - V<sub>EE</sub>, V0 = V<sub>DD</sub> = 5V, V5 = V<sub>EE</sub> = -23V  
V12 = V<sub>DD</sub> - 1/n (V<sub>LCD</sub>), V43 = V<sub>EE</sub> + 1/n (V<sub>LCD</sub>), n = 17(1/240 duty, 1/17 bias)
- V0 = V<sub>DD</sub>, V12 = 3.35V (V<sub>DD</sub> = 5V) or 1.47V (V<sub>DD</sub> = 3V),  
V43 = -21.35V (V<sub>DD</sub> = 5V) or -21.47V (V<sub>DD</sub> = 3V), V5 = V<sub>EE</sub> = -23V, no-load condition (1/240 duty, 1/17 bias)

Single-type mode operation: AMS = V<sub>SS</sub>, SHL = V<sub>SS</sub>

D1\_SID = D3\_DM = V<sub>DD</sub>, D4\_DR = OPEN, ELB = ERB = OPEN,

I<sub>STBY</sub>: V<sub>DD</sub> = 5V, M = V<sub>SS</sub>, D2\_DL = V<sub>SS</sub>, DISOFFB = V<sub>SS</sub>

I<sub>DD</sub>: f<sub>M</sub> = 80Hz, D2\_DL = V<sub>DD</sub>, DISPOFFB = V<sub>DD</sub>

V<sub>DD</sub> = 3 V, display data pattern = 10000000... , 01000000... , 00100000... , 00010000... , ...

V<sub>DD</sub> = 5 V, display data pattern = 10000000... , 01000000... , 00100000... , 00010000... , ...

I<sub>EE</sub>: f<sub>M</sub> = 80Hz, D2\_DL = V<sub>DD</sub>, DISPOFFB = V<sub>DD</sub>

V<sub>DD</sub> = 5V, current through V<sub>EE</sub> Pin, display data pattern = 10000000... , 01000000... , 00100000... , 00010000...

## AC Characteristics

### (1) Segment Driver Application

(V<sub>SS</sub> = 0V, Ta = -30 to +85°C)

Characteristic	Symbol	Test Condition	(1) V <sub>DD</sub> = 5V ± 10%			(2) V <sub>DD</sub> = 3V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t <sub>CY</sub>	Duty = 50%	125	-	-	250	-	-	ns
Clock pulse width	t <sub>WCK</sub>	-	45	-	-	95	-	-	
Clock rise / fall time	t <sub>R</sub> /t <sub>F</sub>	-	-	-	-	-	-	30	
Data set-up time	t <sub>DS</sub>	-	30	-	-	65	-	-	
Data hold time	t <sub>DH</sub>	-	30	-	-	65	-	-	
Clock set-up time	t <sub>CS</sub>	-	80	-	-	120	-	-	
Clock hold time	t <sub>CH</sub>	-	80	-	-	120	-	-	
Propagation delay time	t <sub>PHL</sub>	ELB Output	-	-	60	-	-	125	
		ERB Output	-	-	60	-	-	125	
ELB, ERB set-up time	t <sub>PUS</sub>	ELB Input	30	-	-	65	-	-	
		ERB Input	30	-	-	65	-	-	
DISPOFFB low pulse width	t <sub>WDL</sub>	-	1.2	-	-	1.2	-	-	μs
DISPOFFB clear time	t <sub>CD</sub>	-	100	-	-	100	-	-	ns
M – OUT propagation delay time	t <sub>PD1</sub>	C <sub>L</sub> = 15pF	-	-	1.0	-	-	1.2	μs
CL1 – OUT propagation delay time	t <sub>PD2</sub>		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t <sub>PD3</sub>		-	-	1.0	-	-	1.2	

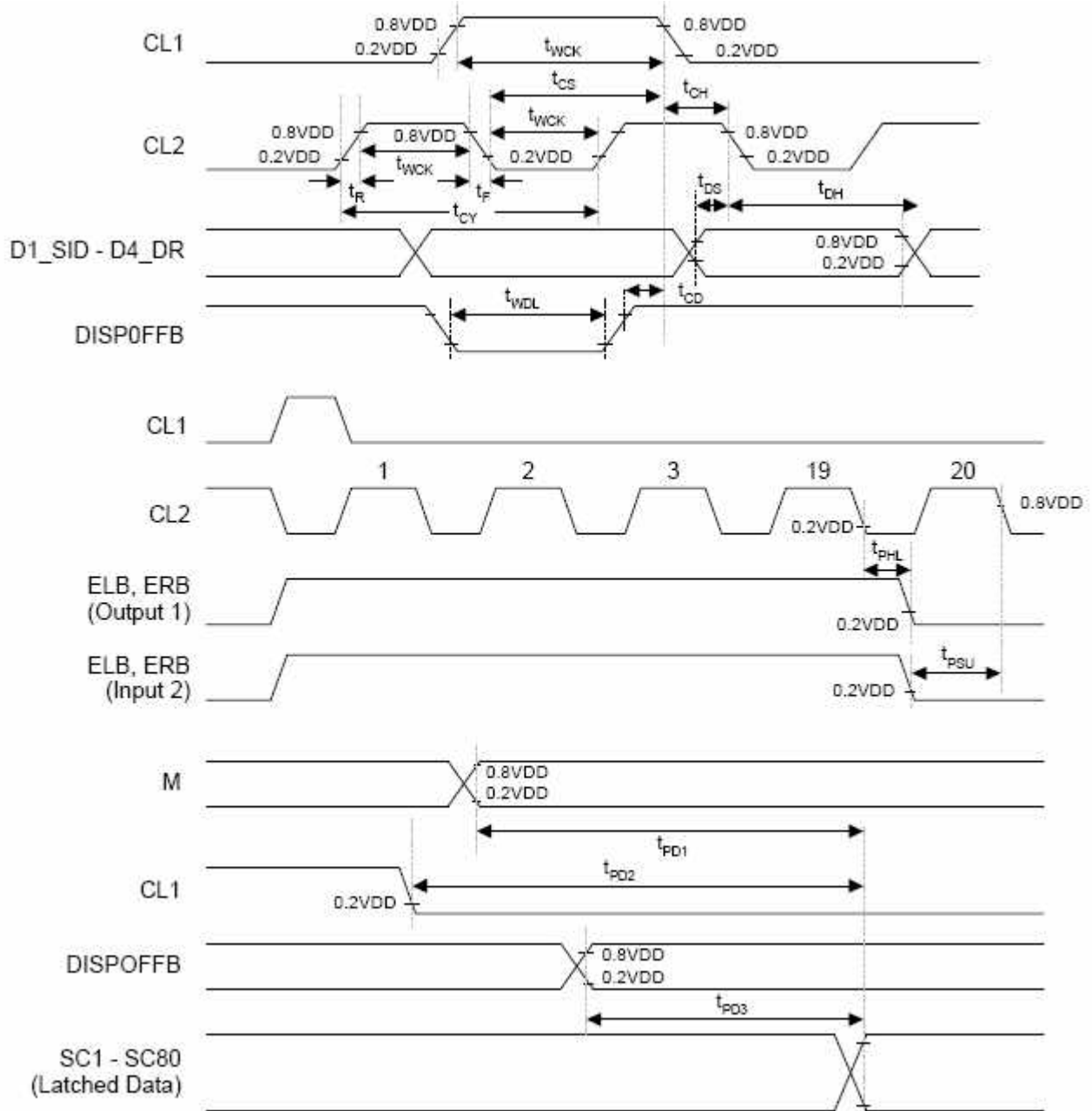
### (2) Common Driver Application

(V<sub>SS</sub> = 0V, Ta = -30 to +85°C)

Characteristic	Symbol	Test Condition	(1) V <sub>DD</sub> = 5V ± 10%			(2) V <sub>DD</sub> = 3V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t <sub>CY</sub>	Duty = 50%	250	-	-	500	-	-	ns
Clock pulse width	t <sub>WCK</sub>	-	45	-	-	95	-	-	
Clock rise / fall time	t <sub>R</sub> /t <sub>F</sub>	-	-	-	50	-	-	50	
Data set-up time	t <sub>DS</sub>	-	30	-	-	65	-	-	
Data hold time	t <sub>DH</sub>	-	30	-	-	65	-	-	
DISPOFFB low pulse width	t <sub>WDL</sub>	-	1.2	-	-	1.2	-	-	μs
DISPOFFB clear time	t <sub>CD</sub>	-	100	-	-	100	-	-	ns
Output delay time	t <sub>DL</sub>	C <sub>L</sub> = 15pF	-	-	200	-	-	250	
M – OUT propagation delay time	t <sub>PD1</sub>		-	-	1.0	-	-	1.2	μs
CL1 – OUT propagation delay time	t <sub>PD2</sub>		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t <sub>PD3</sub>		-	-	1.0	-	-	1.2	

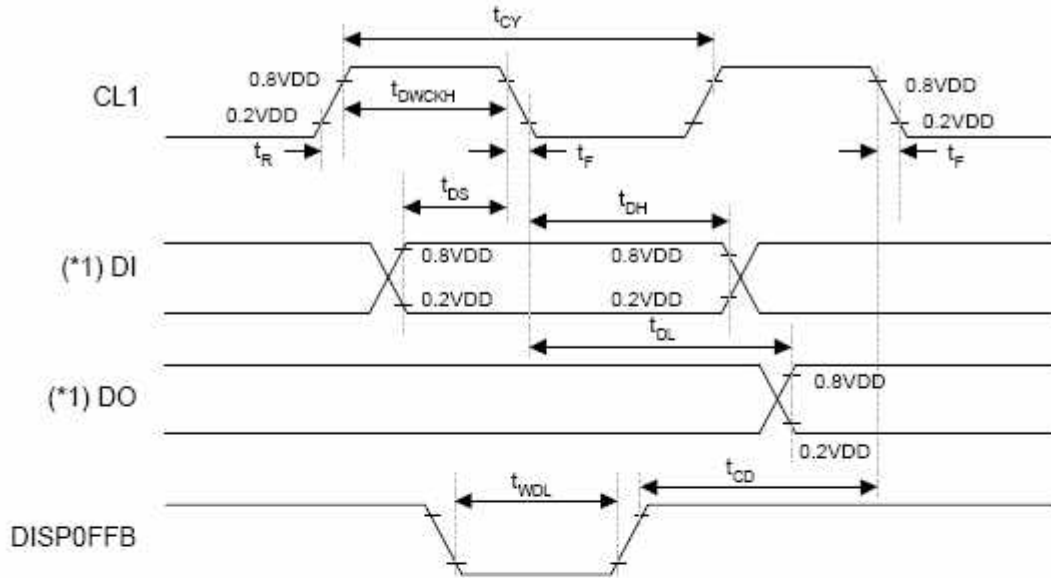
## AC Characteristics (Continued)

### (3) Segment Driver Application Timing

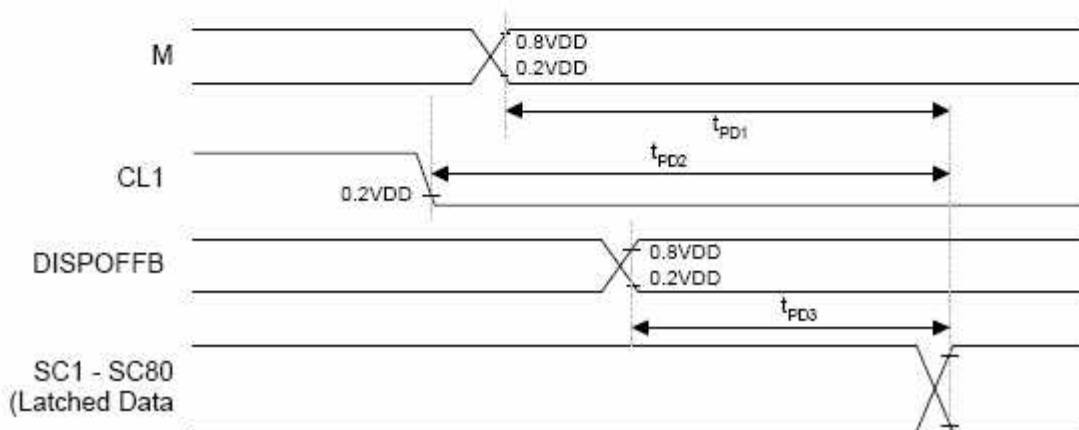


## AC Characteristics (Continued)

### (4) Common Driver Application Timing



(\*1) When in single-type interface mode  
 DI => D2\_DL (SHL = L), D4\_DR (SHL = H)  
 DO => D4\_DR (SHL = L), D2\_DL (SHL = H)  
 When in dual-type interface mode  
 DI => D2\_DL and D3\_DM (SHL = L), D4\_DR and D3\_DM (SHL = H)  
 DO => D4\_DR (SHL = L), D2\_DL (SHL = H)

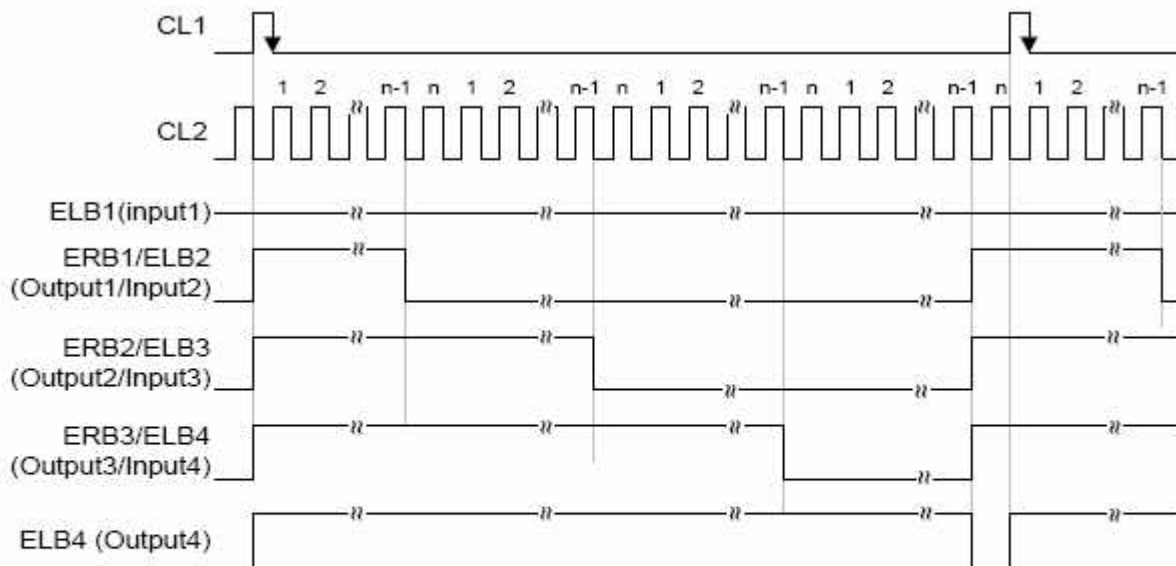


## Power Down Function

In the case of cascade connection of segment mode drivers, SA3086 has a ‘power down function’ in order to reduce the power consumption.

SHL	Enable input	Enable output	Current driver status	The other drivers status
L	ERB	ELB	While ERB = ‘Low’, current driver is enabled.	Disabled
H	ELB	ERB	While ELB = ‘Low’, current driver is enabled.	Disabled

\* In the case of common driver application, power down function does not work.



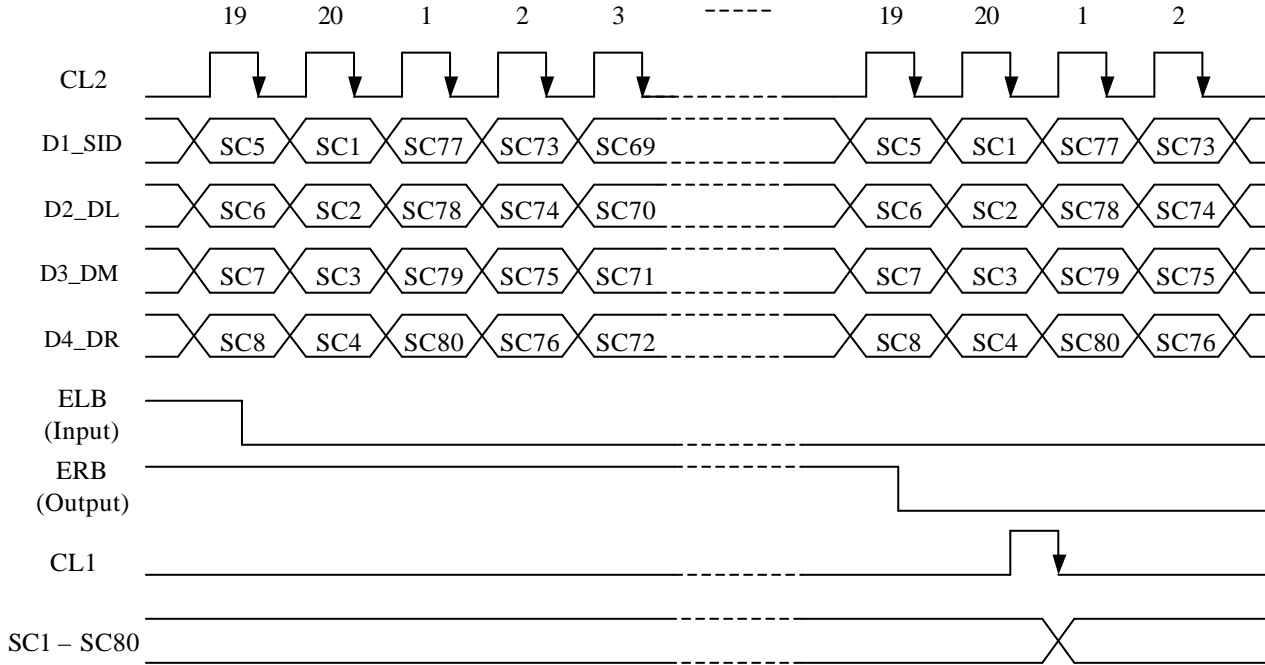
### NOTES:

1. SHL = High (ELB = Input, ERB = Output)  
Current SA3086's ERB must be connected to the next SA3086's ELB.
2. When in 4-bit parallel interface mode: n = 20  
When in 1-bit serial interface mode: n = 80

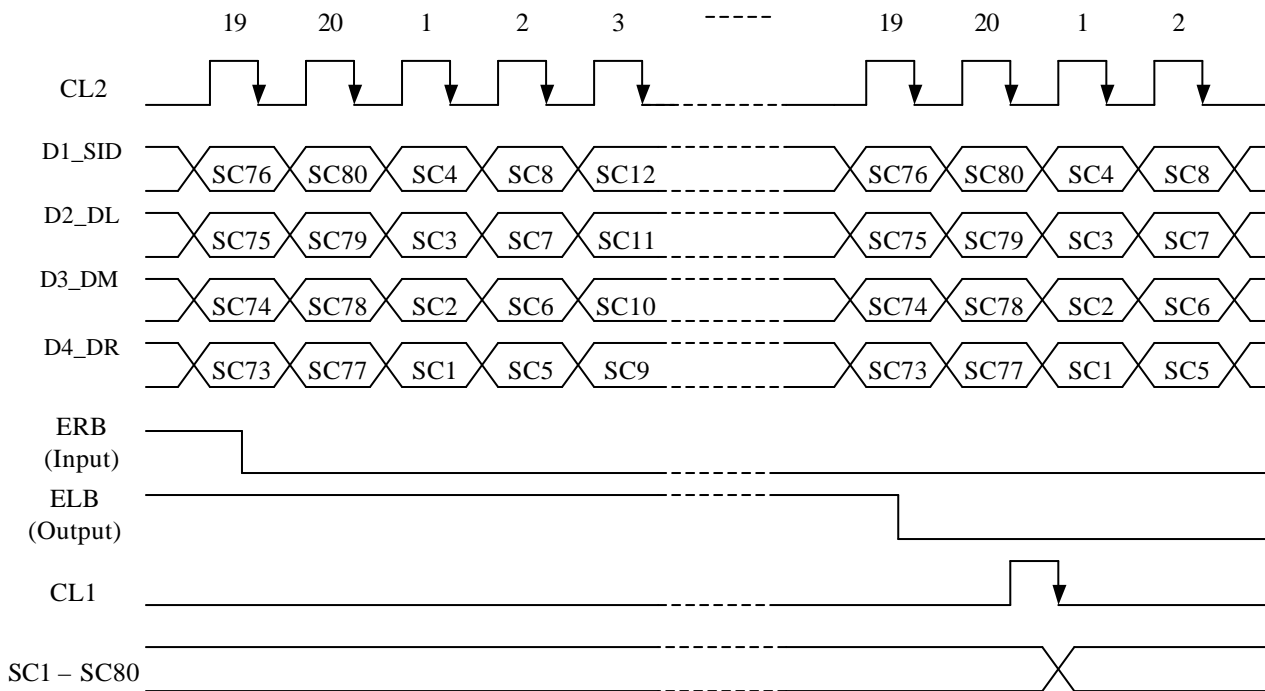
Operation Timing Diagram

(1) 4-BIT Parallel Mode Interface Segment Driver

- When SHL = 'Low'

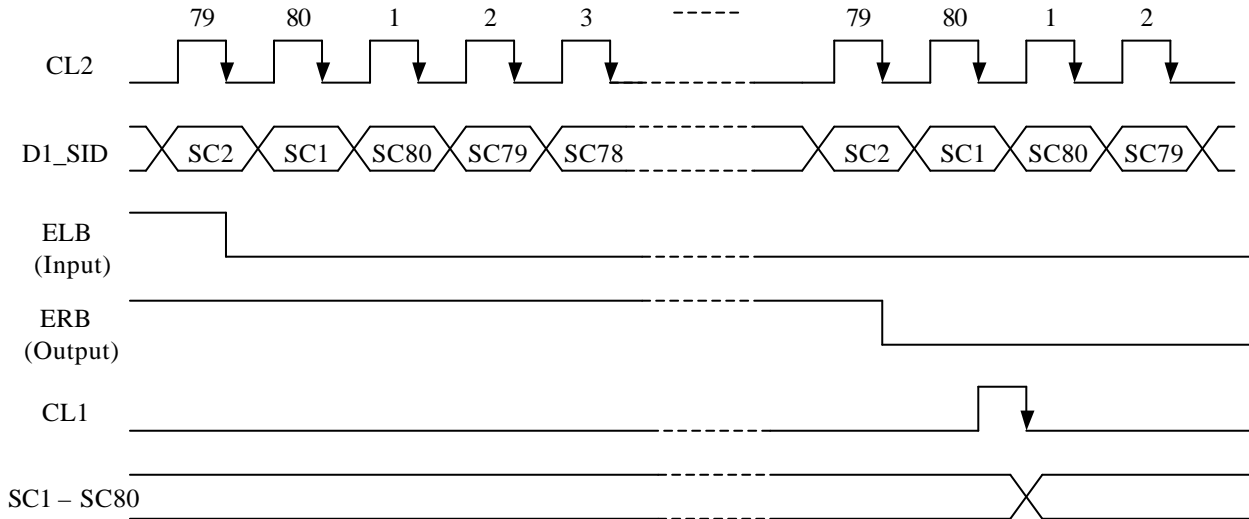


- When SHL = 'High'

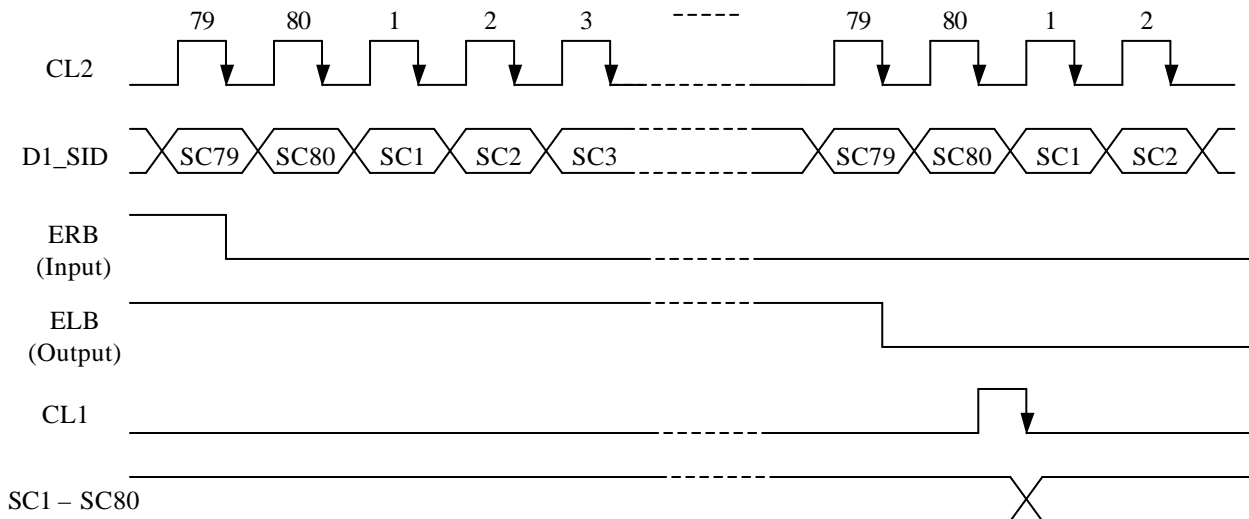


## (2) 1-bit Serial Mode Interface Segment Driver

- When SHL = 'Low'

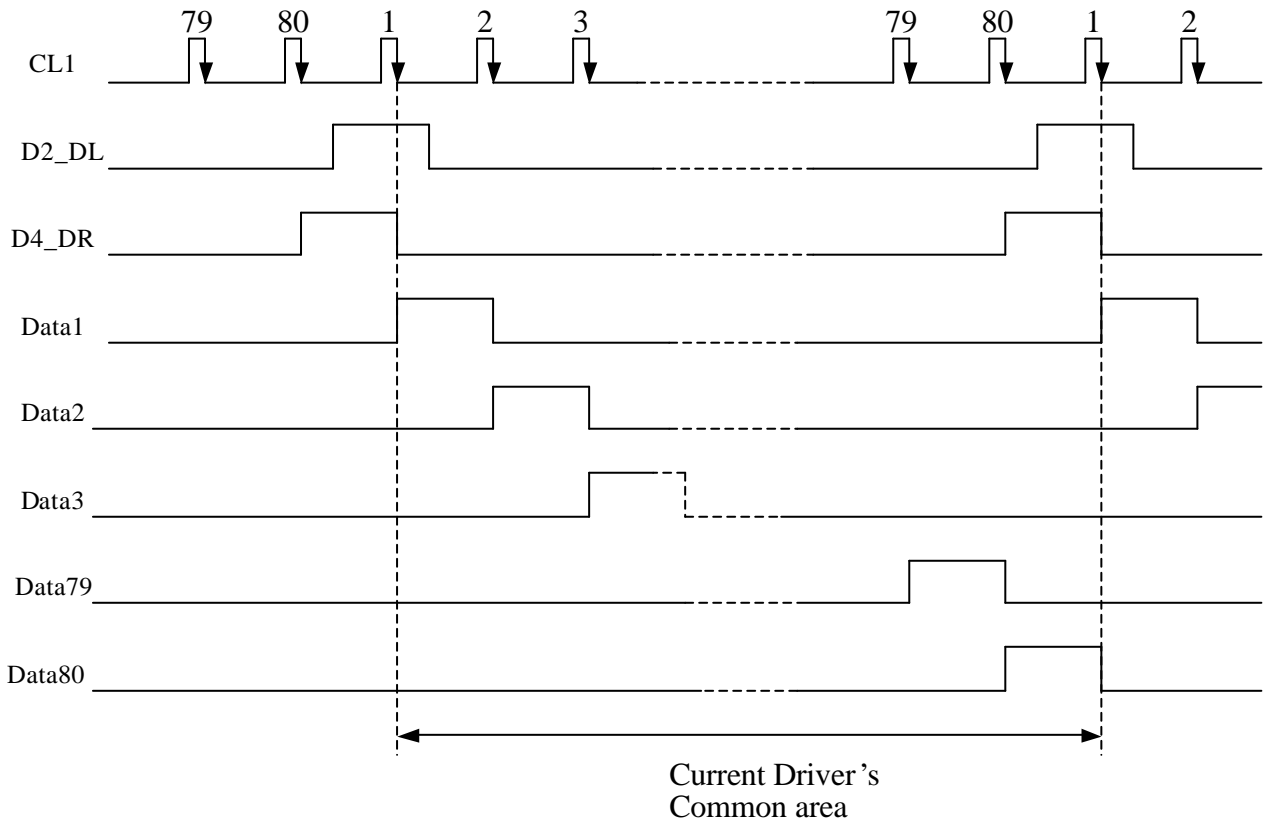


- When SHL = 'High'

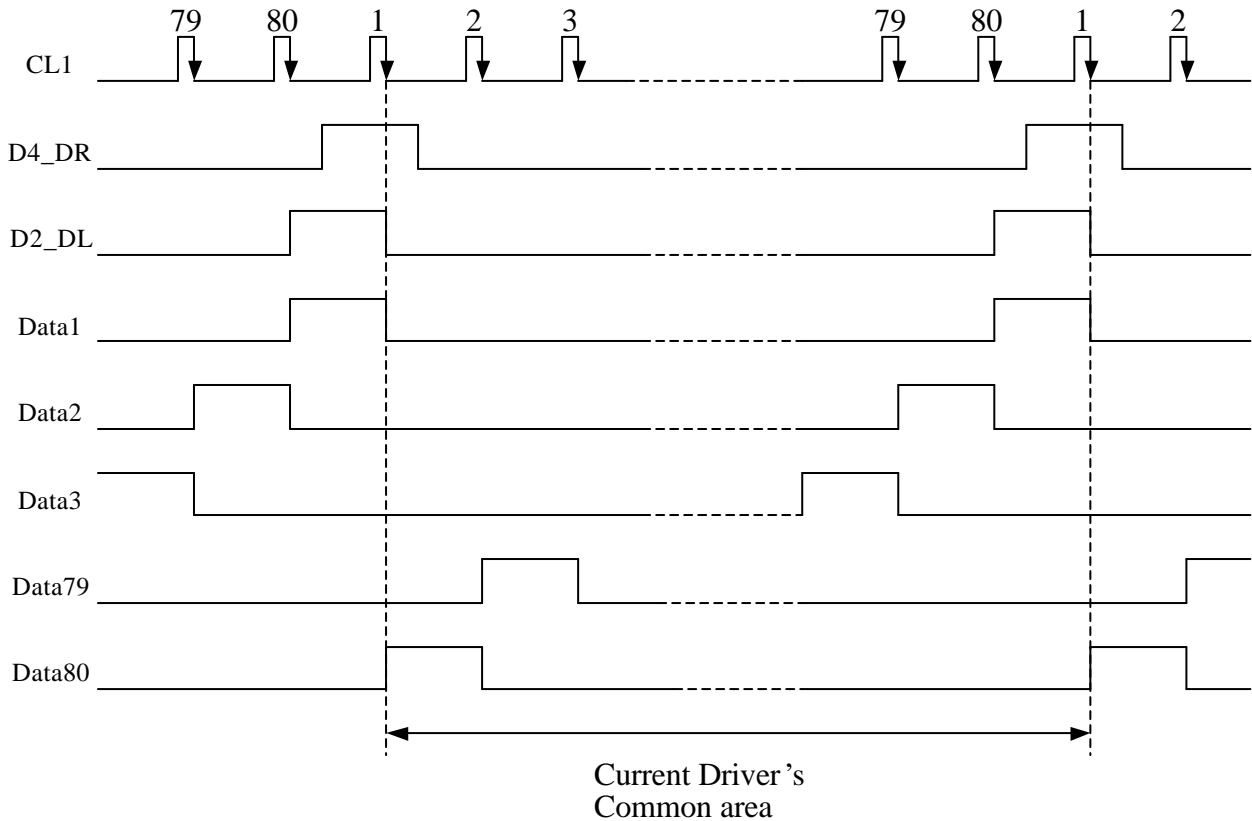


### (3) Single-type Interface Mode Common Driver

- When SHL = 'Low'



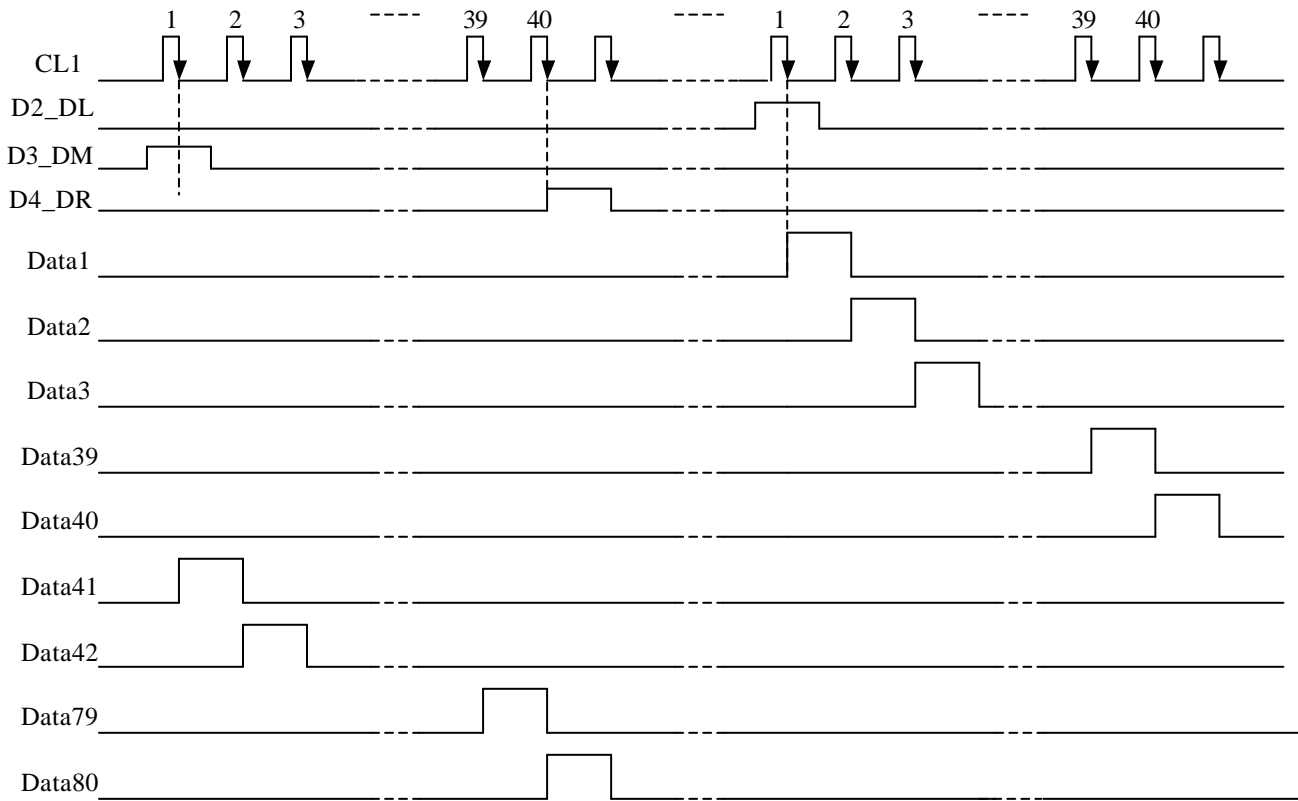
- When SHL = 'High'



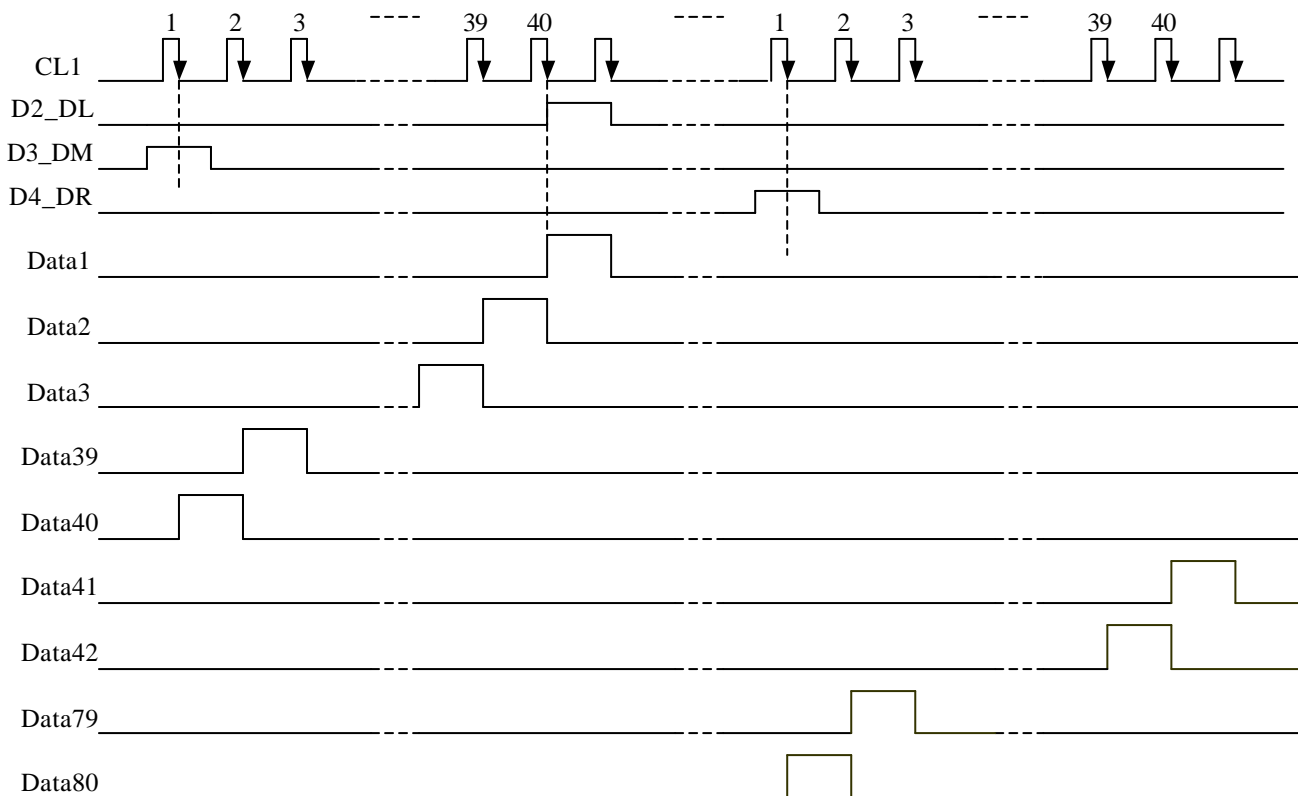


## (4) Dual type interface mode driver

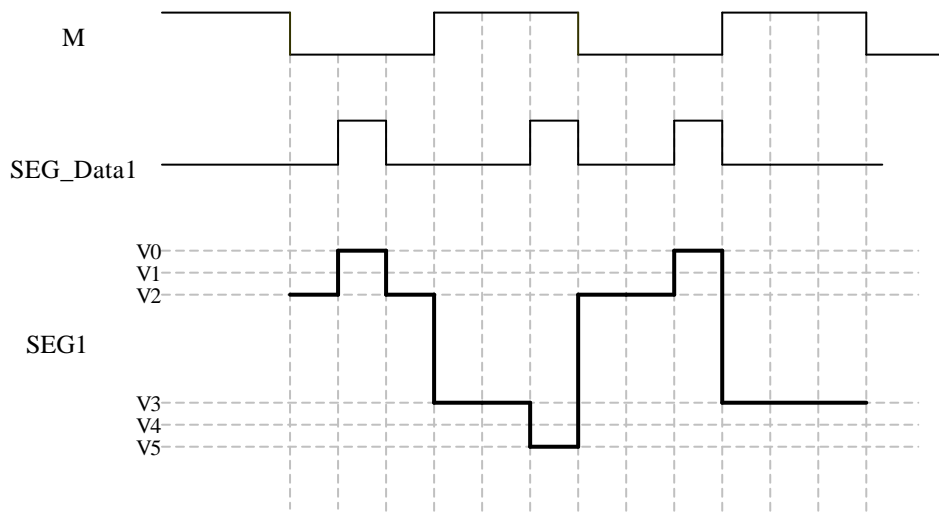
- When SHL = 'Low'



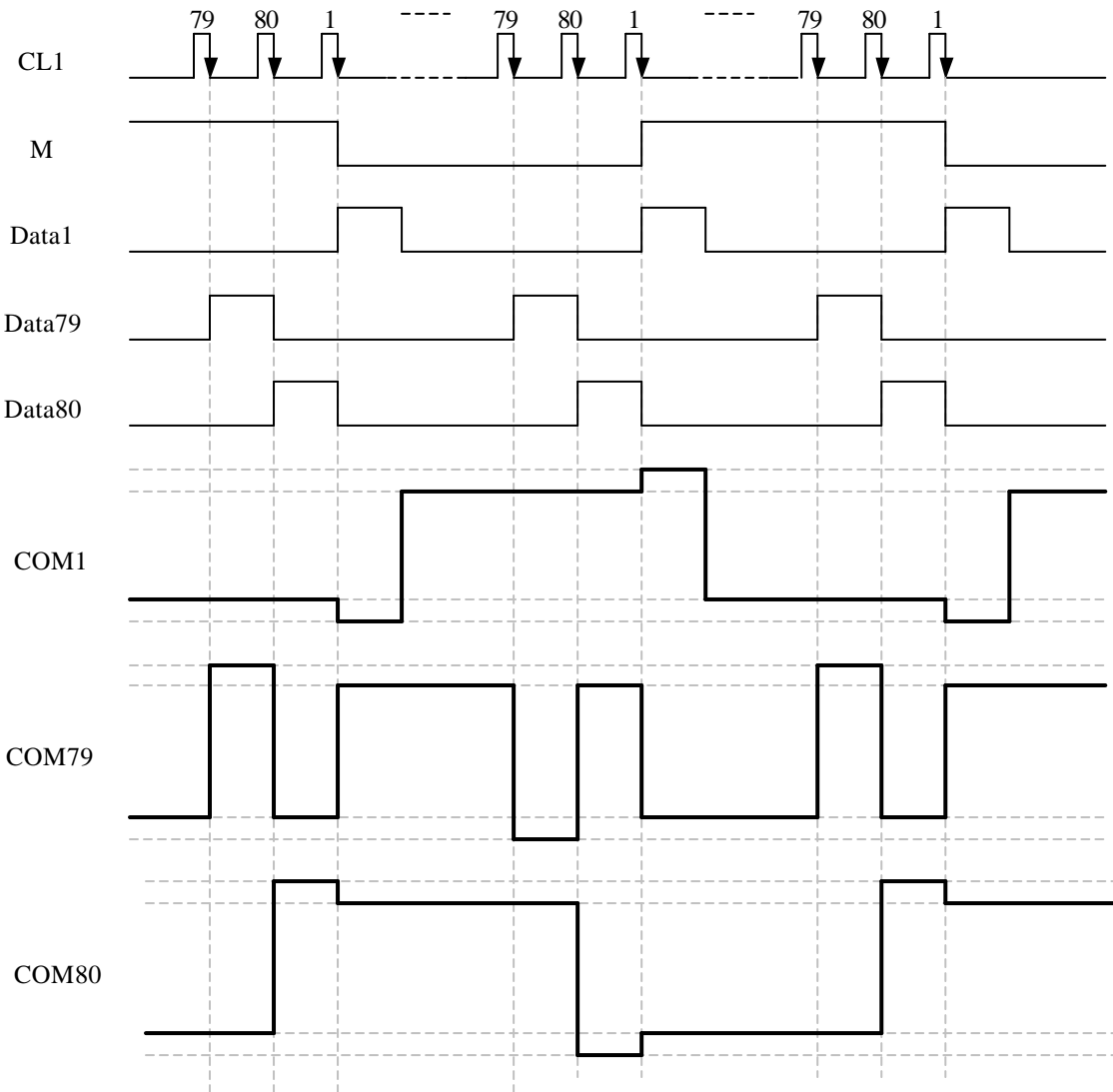
- When SHL = 'High'



(5) Segment Driver Timing



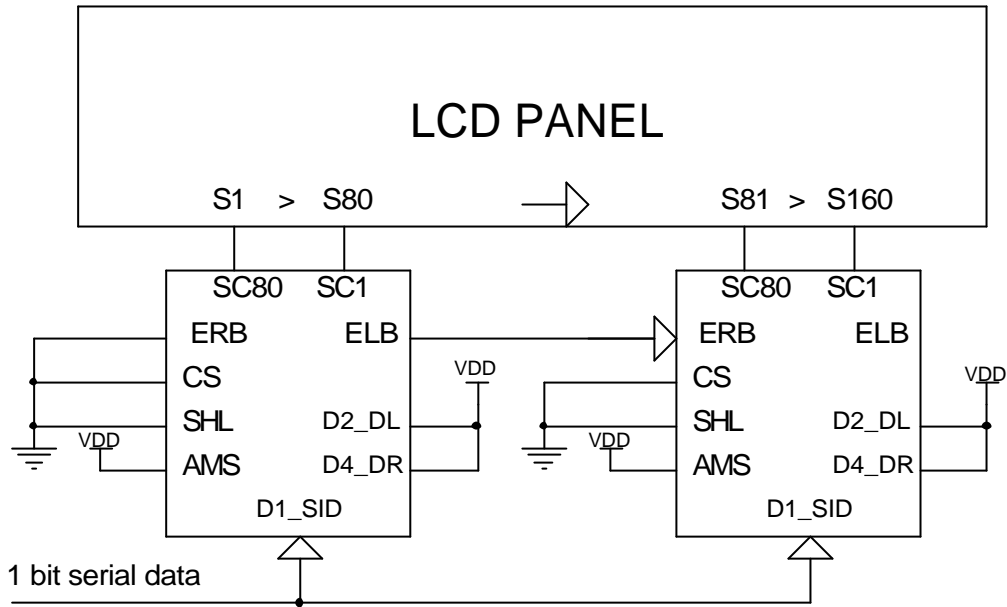
(6) Common Driver Timing



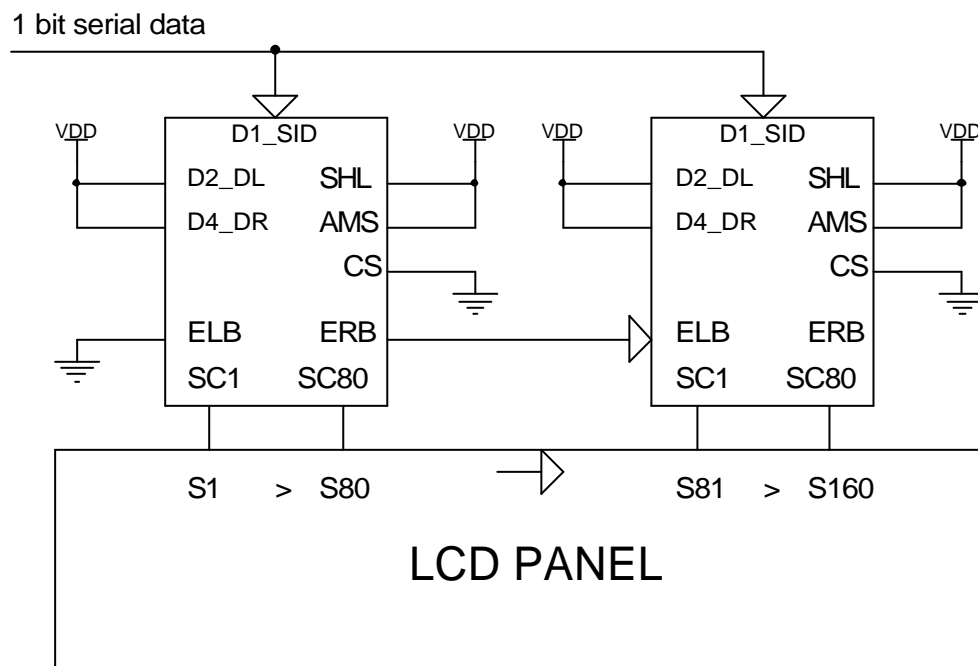
Application Information

1-bit Serial Interface (80-Ch. Segment Driver)

a) Lower View (SHL = L, AMS = H)

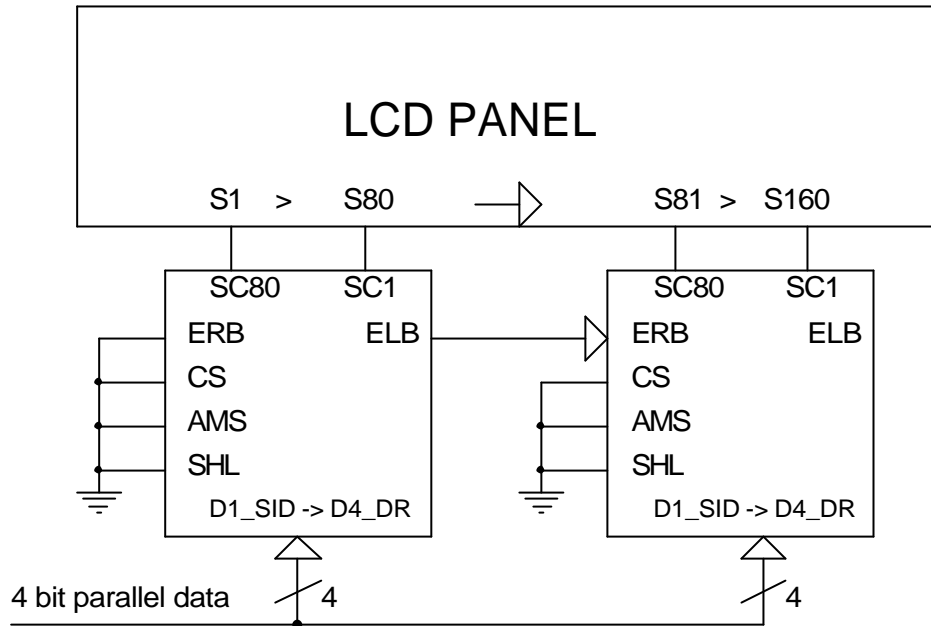


b) Upper View (SHL = H, AMS = H)

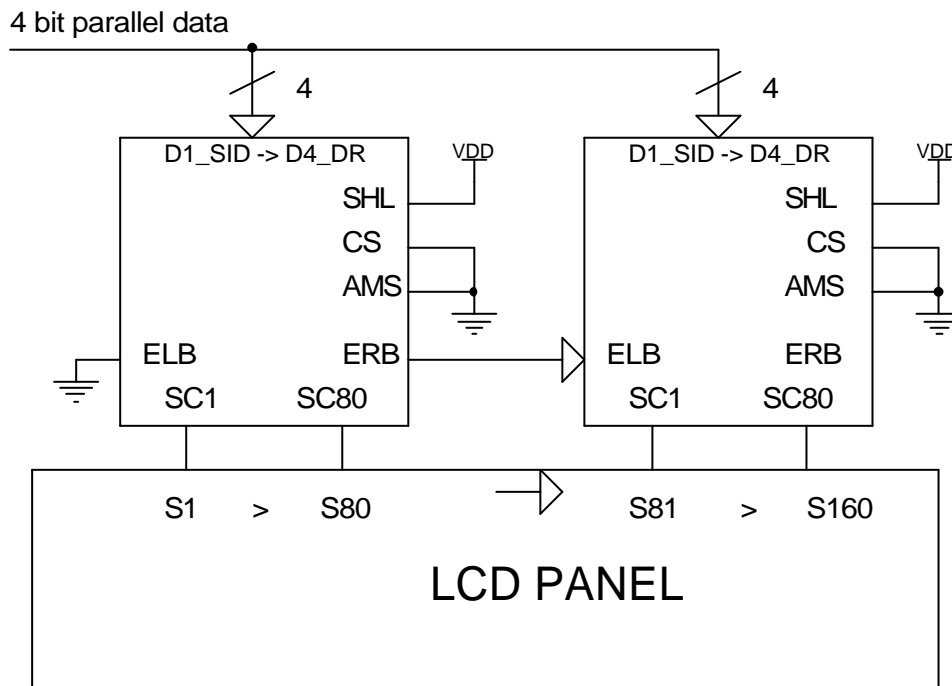


4-Bit Parallel Interface Mode (80 Ch. Segment Driver)

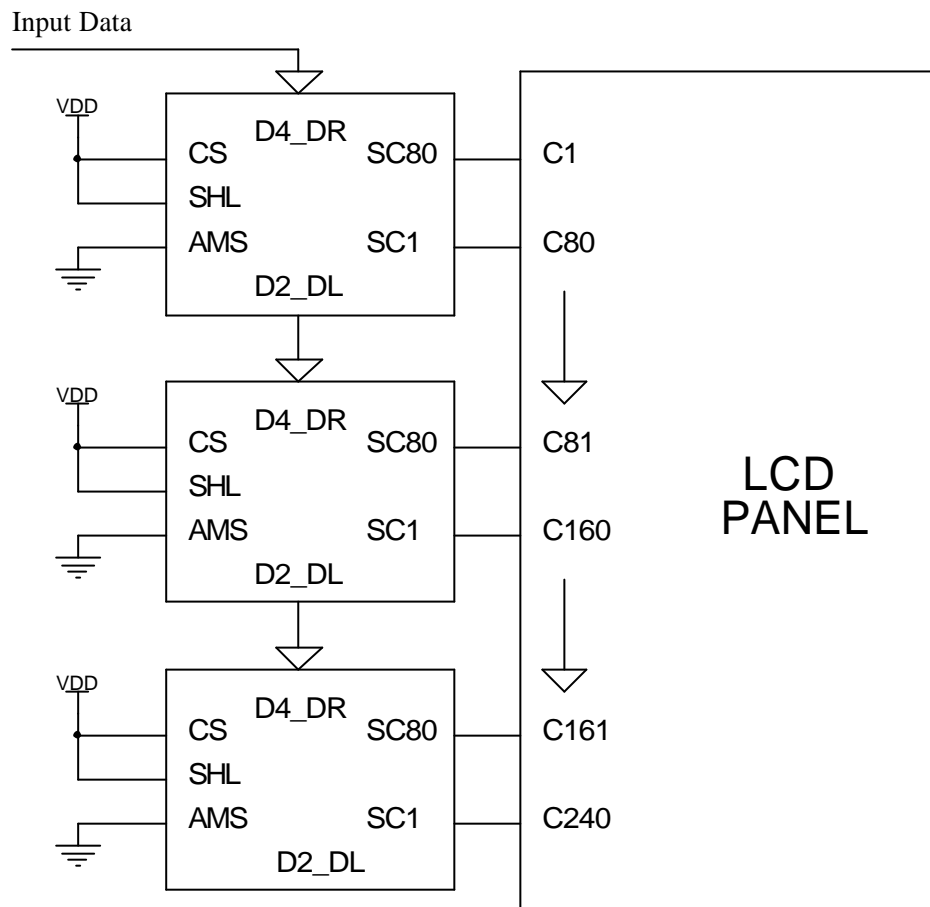
a) Lower View (SHL = L, AMS = L)



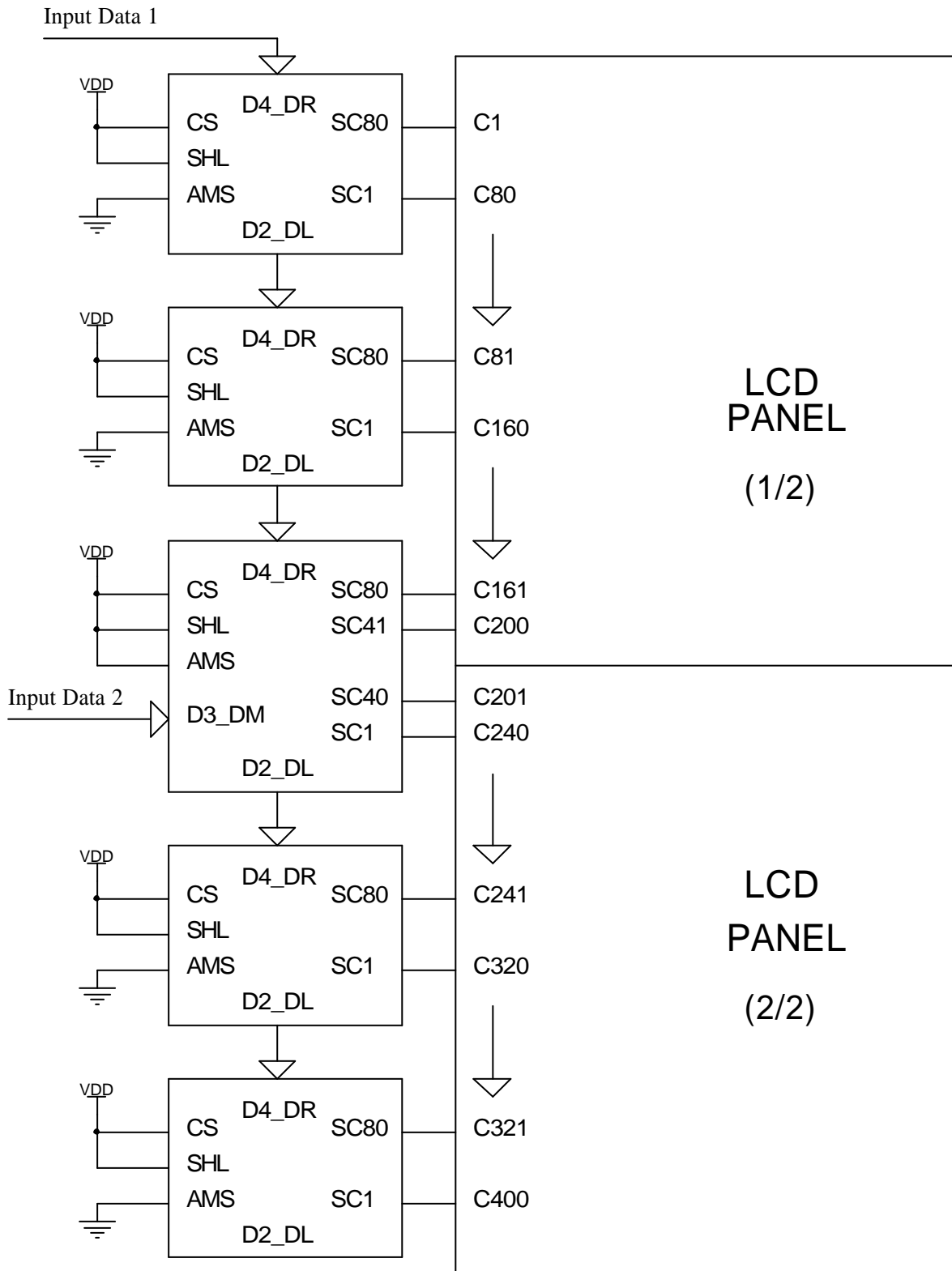
b) Upper View (SHL = H, AMS = L)



## Single-type Interface Mode (80 Ch. Common Driver)



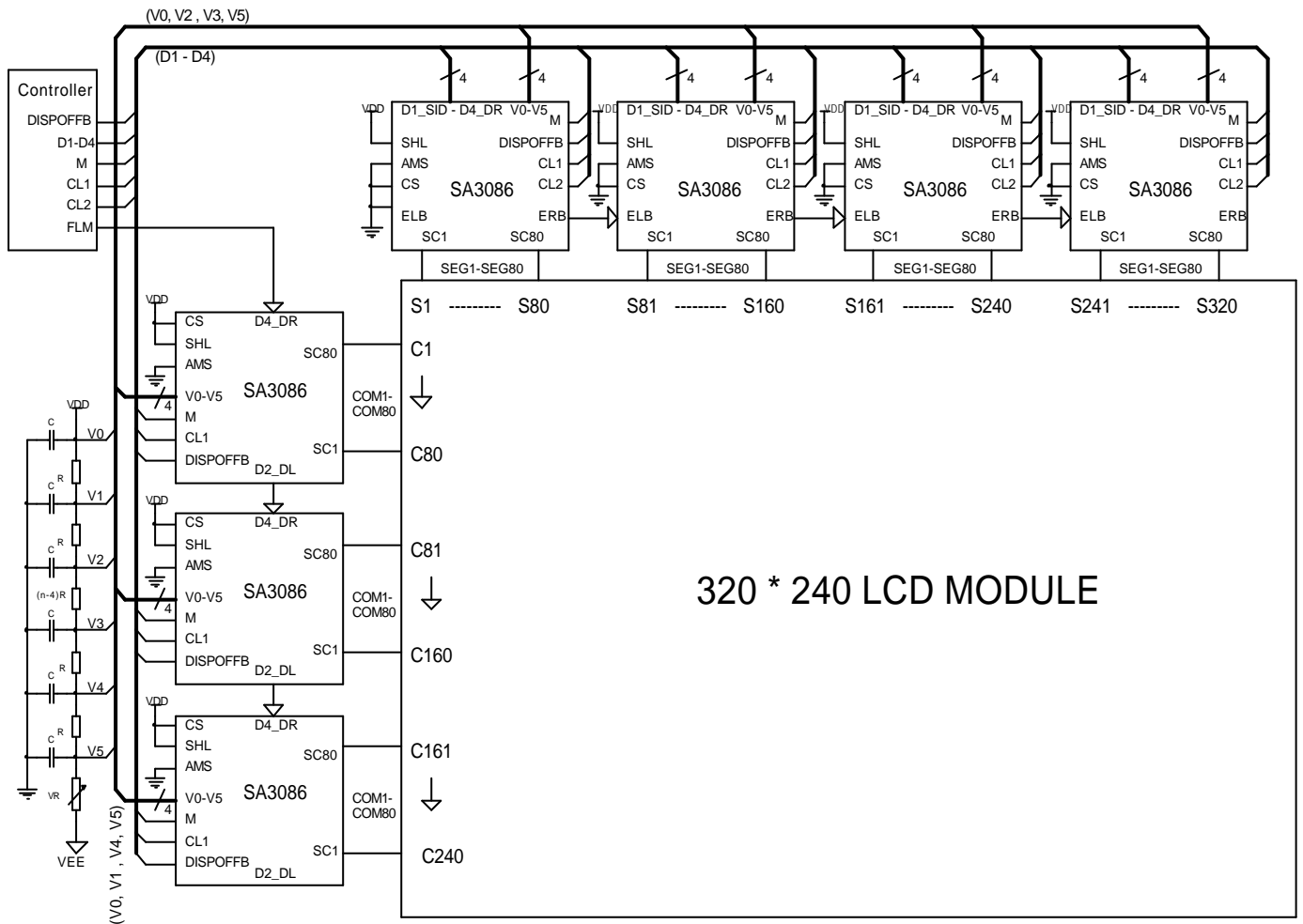
## Dual-type Interface Mode (40 Ch. Common Driver)



**Note:** Using this application mode (dual-type common mode), the duty ratio can be reduced to half, in case, 1/200 duty can be used to drive the 400 common LCD panel.

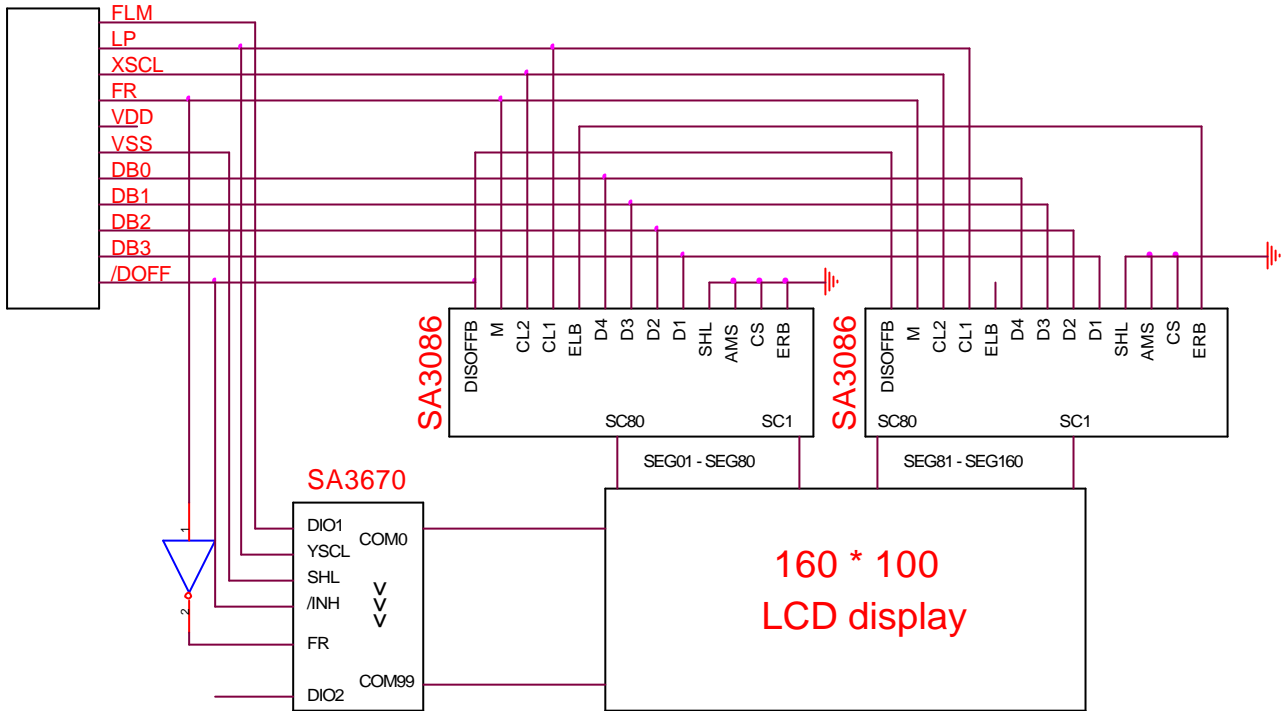
## Application Circuit Example (1)

Using SA3086 for 320 x 240



## Application Circuit Example (2)

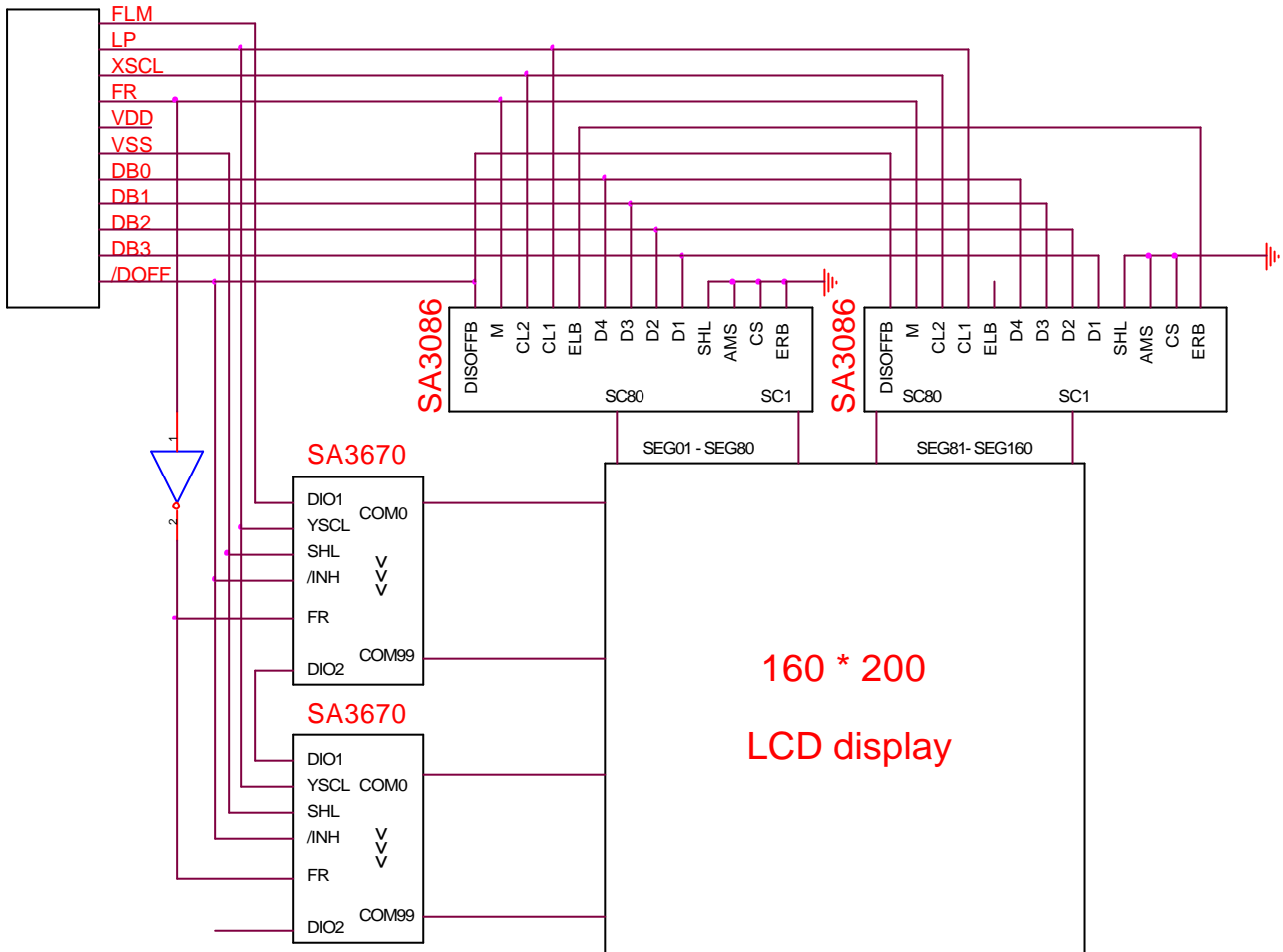
Using SA3086 with SA3670 (160 \* 100)





## Application Circuit Example (3)

Using SA3086 with SA3670 (160 \* 200)



### Remark:

Wedge tool : ASM-1820-L DSR (004x010) W=003

Bonding wire : 1.0mil or 25um

	Power (mW)	Time (ms)	Force (gf)
ASM559	75-85	20	20
ASM520	75-85	20	20