SA3080

80 CHANNEL SEGMENT DRIVER FOR DOT MATRIX LCD

Technical Specification

Hong Kong Office

Room C, 19/F, Ritz Plaza,
122 Austin Road, Tsim Sha Tsui,
Kowloon, Hong Kong

Tel: (852) 2622 2055
Fax: (852) 2622 2117

China Tel: (86) 755-6117 8231
China Fax:(86) 755-6117 8393

Web site: http://www.redwood.hk/

Introduction

SA3080 is a low cost 80-channel segment LCD driver IC that fabricated by low power CMOS technology. This IC is used together SA3086 for 80 x 80, 160 x 80 and 240 x 80 dot matrix display. It can also be used with SA3670 for 80 x 100, 160 x 100, 240 x 100 displays. Interface with LCD controller is 1-bit serial.

Features

- Low power CMOS process.
- Dot matrix LCD driver with 80-channel output.
- Serial display data and control signal from the controller LSI.
- Display driving bias: static ~ 1/10.
- Power supply voltage: 2.7- 5.5V.
- Max. supply voltage for display: 13.0V ($V_{LCD} = V_{DD} - V_{EE}$).
- Serial interface with LCD controller.

Configuration	Segment driver	Common driver
80 x 80	1 pc of SA3080	1 pc of SA3086
160 x 80	2 pcs of SA3080	1 pc of SA3086
240 x 80	3 pcs of SA3080	1 pc of SA3086
80 x 100	1 pc of SA3080	1 pc of SA3670
160 x 100	2 pc of SA3080	1 pc of SA3670
240 x 100	3 pc of SA3080	1 pc of SA3670

Block Diagram

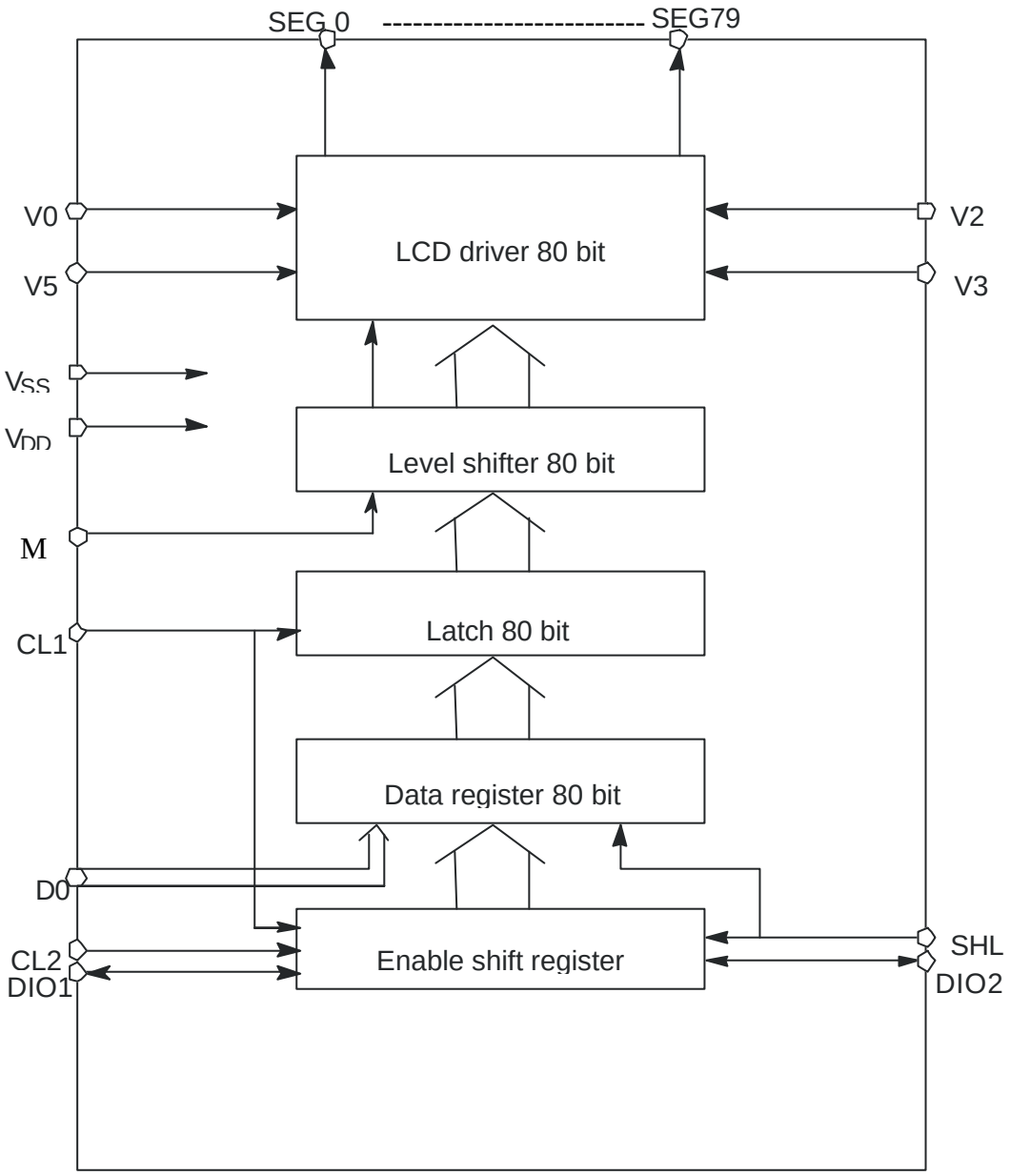
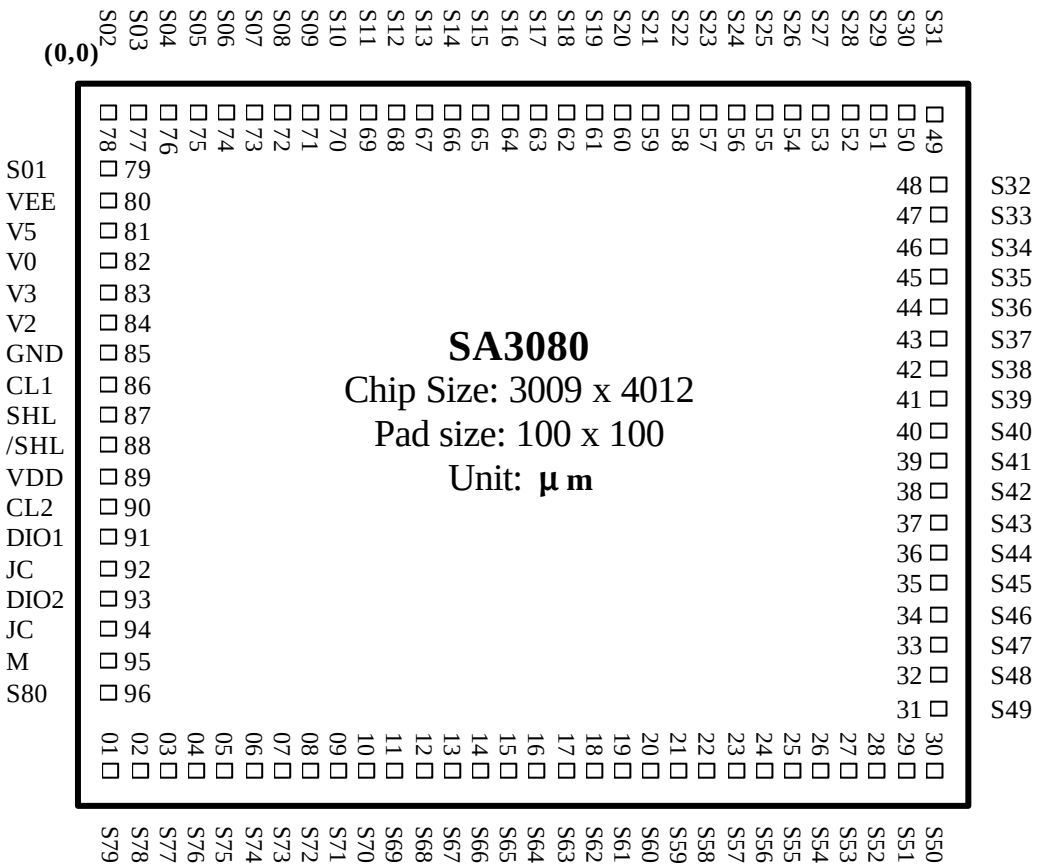


Figure 1. Block Diagram

Pad Diagram



Substrate should be connect VDD or floating

Pad Coordinates

PAD NUM.	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUM.	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUM.	PAD NAME	COORDINATE X	COORDINATE Y
1	S79	2860.00	157.25	33	S47	2333.25	3867.50	65	S15	148.75	1814.75
2	S78	2860.00	284.75	34	S46	2205.75	3867.50	66	S14	148.75	1687.25
3	S76	2860.00	412.25	35	S45	2078.25	3867.50	67	S13	148.75	1559.75
4	S75	2860.00	539.75	36	S44	1950.75	3867.50	68	S12	148.75	1432.25
5	S74	2860.00	667.25	37	S43	1823.25	3867.50	69	S11	148.75	1304.75
6	S73	2860.00	794.75	38	S42	1695.75	3867.50	70	S10	148.75	1177.25
7	S72	2860.00	922.25	39	S41	1568.25	3867.50	71	S09	148.75	1049.75
8	S71	2860.00	1049.75	40	S40	1440.75	3867.50	72	S08	148.75	922.25
9	S70	2860.00	1177.25	41	S39	1313.25	3867.50	73	S07	148.75	794.75
10	S69	2860.00	1304.75	42	S38	1185.75	3867.50	74	S06	148.75	667.25
11	S68	2860.00	1432.25	43	S37	1058.25	3867.50	75	S05	148.75	539.75
12	S67	2860.00	1559.75	44	S36	930.75	3867.50	76	S04	148.75	412.25
13	S66	2860.00	1687.25	45	S35	803.25	3867.50	77	S03	148.75	284.75
14	S65	2860.00	1814.75	46	S34	675.75	3867.50	78	S02	148.75	157.25
15	S64	2860.00	1942.25	47	S33	548.25	3867.50	79	S01	403.75	144.50
16	S63	2860.00	2069.75	48	S32	420.75	3867.50	80	VEE	531.25	144.50
17	S62	2860.00	2197.25	49	S31	148.75	3854.75	81	V5	658.75	144.50
18	S61	2860.00	2324.75	50	S30	148.75	3727.25	82	V0	786.25	144.50
19	S60	2860.00	2452.25	51	S29	148.75	3599.75	83	V3	913.75	144.50
20	S59	2860.00	2579.75	52	S28	148.75	3472.25	84	V2	1041.25	144.50
21	S58	2860.00	2707.25	53	S27	148.75	3344.75	85	GND	1168.75	144.50
22	S57	2860.00	2834.75	54	S26	148.75	3217.25	86	CL1	1313.25	144.50
23	S56	2860.00	2962.25	55	S25	148.75	3089.75	87	SHL	1440.75	144.50
24	S55	2860.00	3089.75	56	S24	148.75	2962.25	88	/SHL	1568.25	144.50
25	S54	2860.00	3217.25	57	S23	148.75	2834.75	89	VDD	1695.75	144.50
26	S53	2860.00	3344.75	58	S22	148.75	2707.75	90	CL2	1823.25	144.50
27	S52	2860.00	3472.25	59	S21	148.75	2579.75	91	DIO1	1950.75	144.50
28	S51	2860.00	3599.75	60	S20	148.75	2452.25	92	JC	2078.25	144.50
29	S50	2860.00	3727.25	61	S19	148.75	2324.75	93	DIO2	2205.75	144.50
30	S49	2860.00	3854.75	62	S18	148.75	2197.25	94	JC	2333.25	144.50
31	S48	2588.25	3867.50	63	S17	148.75	2069.75	95	M	2460.75	144.50
32	S47	2460.75	3867.50	64	S16	148.75	1942.25	96	S80	2605.25	144.50

Pin Descption

<table>
<tr><th>Pin (No.)</th><th>I/O</th><th>Name</th><th>Description</th><th>Interface</th></tr>
<tr><td>V_{DD} (40)</td><td rowspan="3">Power</td><td rowspan="2">Operating Voltage</td><td>For logical circuit (2.7 - 5.5V)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>V_{SS} GND (36)</td><td>0V (GND)</td></tr>
<tr><td>V_{EE} (31)</td><td>Negative Supply Voltage</td><td>For LCD driver circuit</td></tr>
<tr><td>V0, V5 (33, 32)</td><td>I</td><td rowspan="2">LCD driver output voltage level</td><td>Bias voltage level for LCD drive (select level)</td><td rowspan="2">Power</td></tr>
<tr><td>V2, V3 (35, 34)</td><td>I</td><td>Bias voltage level for LCD drive (Non-select level)</td></tr>
<tr><td>SHL /SHL (38,39)</td><td>I</td><td>LCD driver Data interface</td><td>Selection of the shift direction of shift register
<table><tr><th>SHL</th><th>/SHL</th><th>DIO1</th><th>DIO2</th></tr><tr><td>V_{DD}</td><td>V_{SS}</td><td>Out</td><td>In</td></tr><tr><td>V_{SS}</td><td>V_{DD}</td><td>In</td><td>Out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DIO1 (42)</td><td>I/O</td><td rowspan="2">LCD driver Data interface</td><td rowspan="2">Data input/output of shift register</td><td rowspan="2">Controller or SA3080</td></tr>
<tr><td>DIO2 (44)</td><td>I/O</td></tr>
<tr><td>S01- S80</td><td>O</td><td>Driver Output</td><td>LCD Driver Segment Output</td><td>LCD</td></tr>
<tr><td>M (46)</td><td>I</td><td>Alternated signal for LCD driver output</td><td>The alternating signal to convert LCD drive waveform to AC</td><td rowspan="2">Controller</td></tr>
<tr><td>CL1, CL2 (37,41)</td><td>I</td><td>Data shift / Latch clock</td><td>CL1: Data latch clock
CL2: Data shift clock</td></tr>
</table>

Data Shift Direction

SHL	/SHL	Data Direction
0	1	S80→S01
1	0	S01→S80

Maximum Absolute Limit (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3 to +7.0	V
Driver Supply Voltage	V_{LCD}	V_{DD}- 15.0 to V_{DD} + 0.3	V
Input Voltage 1	V_{IN1}	-0.3 to V_{DD} + 0.3	V
Input Voltage 2 ($V_1 – V_4$)	V_{IN2}	V_{DD} + 0.3 to V_{EE} - 0.3	V
Operating Temperature	T_{OPR}	- 30 to + 85	°C
Storage Temperature	T_{SRG}	-55 to + 125	°C

* Voltage greater than above may damage the circuit
* V_{EE}: connect a protection resistor (220Ω± 5%)

Electrical Characterstics

DC Characteristics (V_{DD} = 2.7 - 5.5V, V_{DD}-V_{EE} = 3 - 13V, V_{SS} = 0V, Ta = -30 - +85°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current *	I_{DD}	f_{CL2} = 400kHz	-	1	mA	-
Supply Current *	I_{EE}	f_{CL1}=1kHz	-	10	µA	
Input High Voltage	V_{IH}	-	0.7V_{DD}	V_{DD}	V	CL1, CL2, DIO1, DIO2, SHL, /SHL, FR,
Input Low Voltage	V_{IL}		0	0.3V_{DD}		
Input Leakage Current	I_{LKG}	V_{IN} = 0-V_{DD}	-5	5	µA	
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	V_{DD}-0.4	-	V	DIO1, DIO2
Output Low Voltage	V_{OL}	I_{OL} = +0.4mA	-	0.4		
Voltage Descending	V_{D1}	I_{ON} = 0.1mA for one of S1-S80	-	1.1		V (V0, V2, V3, V5) S (S01-S80)
	V_{D2}	I_{ON} = 0.05mA for each S1-S80	-	1.5 *		
Leakage Current	I_V	V_{IN} = V_{DD}-V_{EE} (Output S1~S80: floating)	-10	10	µA	V0, V2, V3, V5

* The parameter is guaranteed.

AC Characteristics (V_{DD} = 2.7 to 5.5V, V_{DD}-V_{EE} = 3 to 13V, V_{SS} = 0V, Ta = -30 to +85 °C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f_{CL}	-	-	400	kHz	CL2
Clock High Level Width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	-	800	-		CL2
Clock Set-up Time	t_{SL}	From CL2 to CL1	500	-		CL1, CL2
	t_{LS}	From CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R/t_F	-	-	200		
Data Set-up Time	t_{SU}	-	300	-		DIO1, DIO2
Data Hold Time	t_{DH}	-	300	-		
Data Delay Time	t_D	C_L = 15pF	-	500		

- Input/Output current is excluded; when input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, to avoid this, input level must be fixed at "H" or "L".

Timing Characteristics

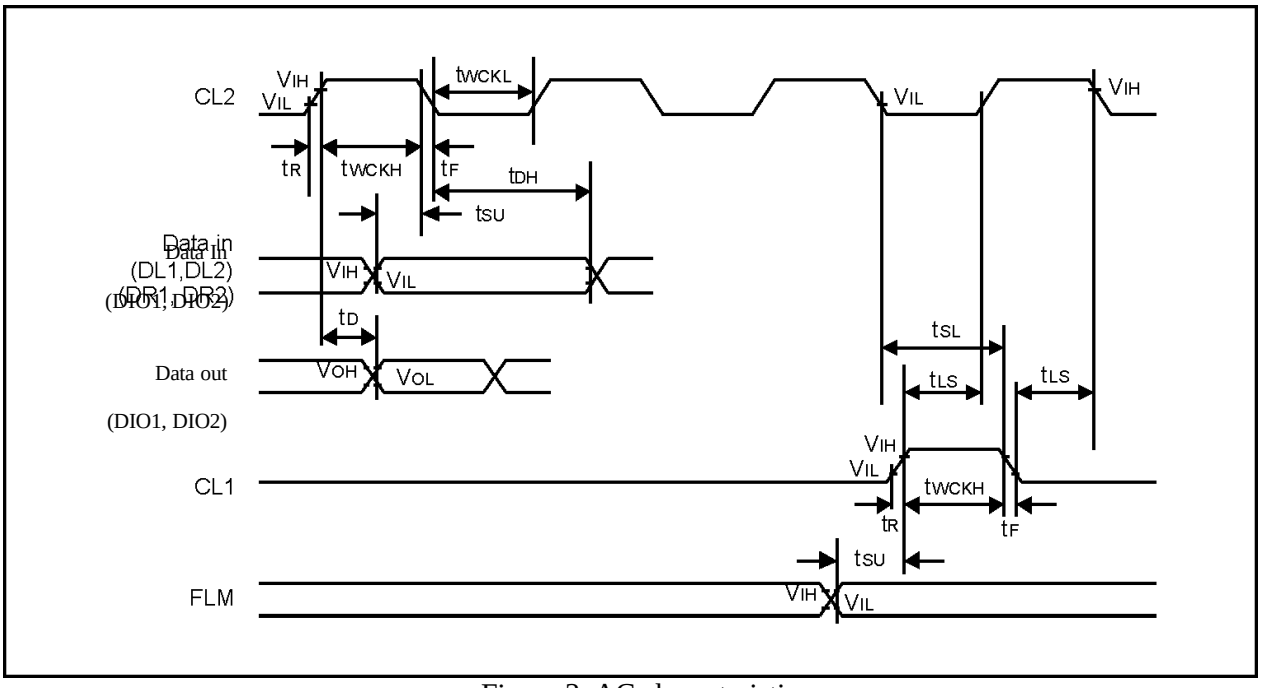


Figure 3. AC characteristics

LCD OUTPUT WAVEFORMS

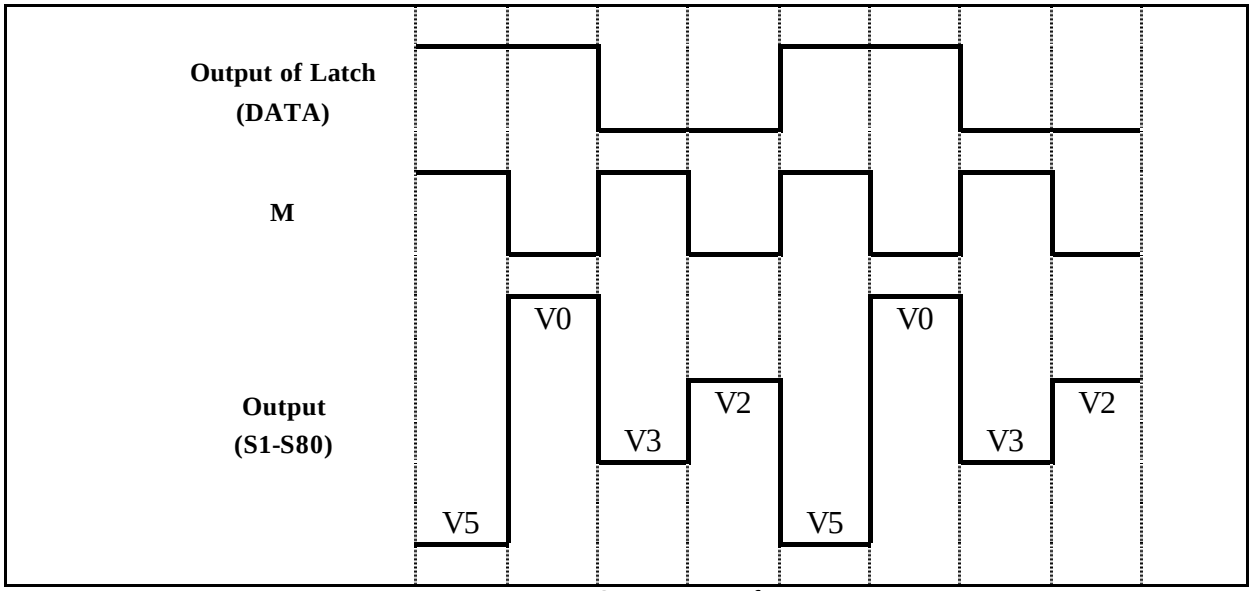
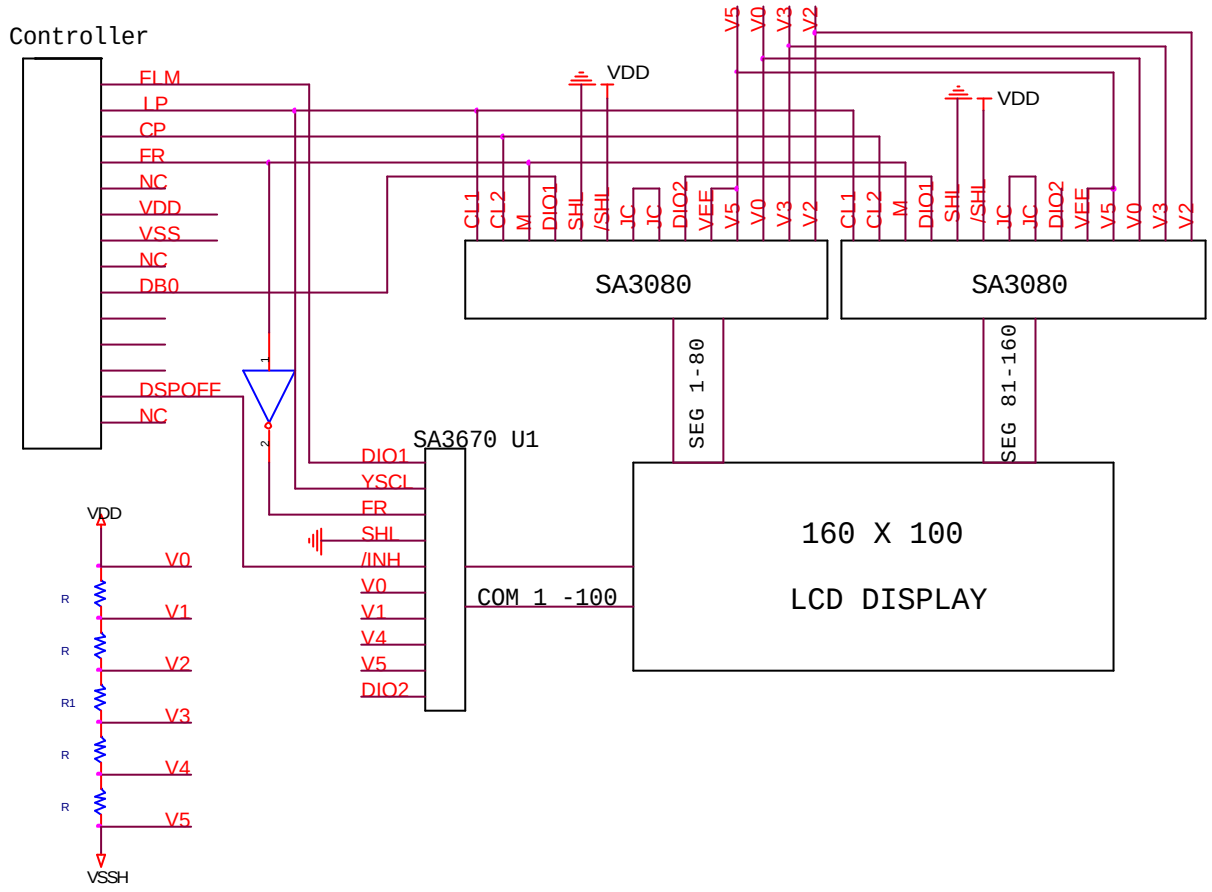


Figure 4. Output Waveforms

APPLICATION CIRCUIT (1)

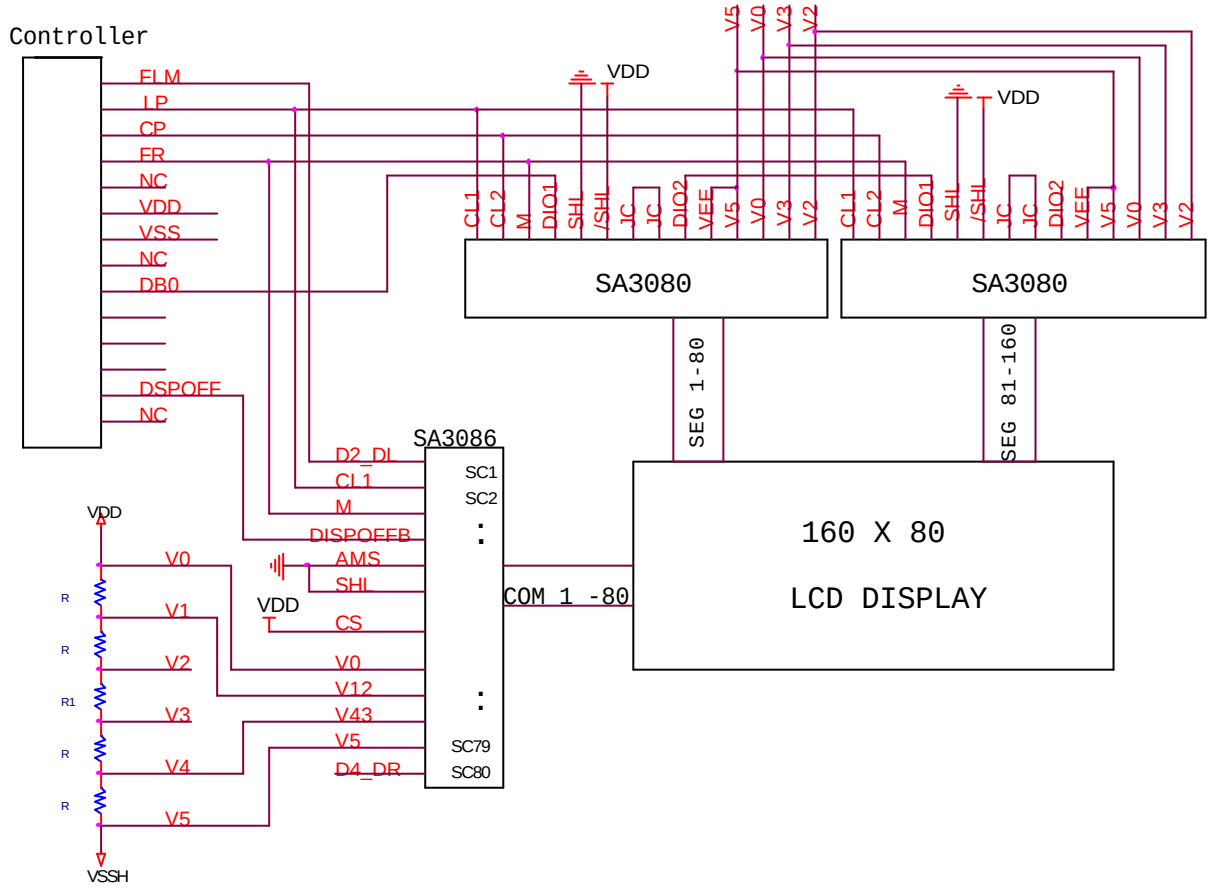
160 * 100 LCD Display SA3670 combination with SA3080



Data flow direction: The LCD display segment data direction is S160 to S01

APPLICATION CIRCUIT (2)

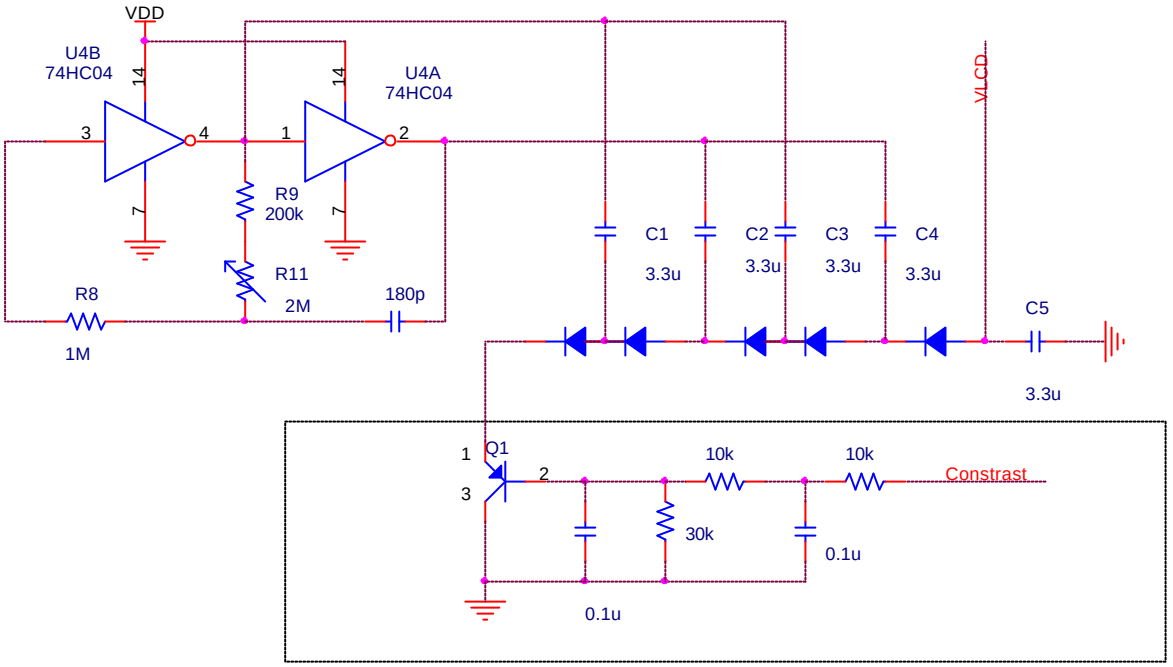
160 * 80 LCD Display SA3086 combination with SA3080



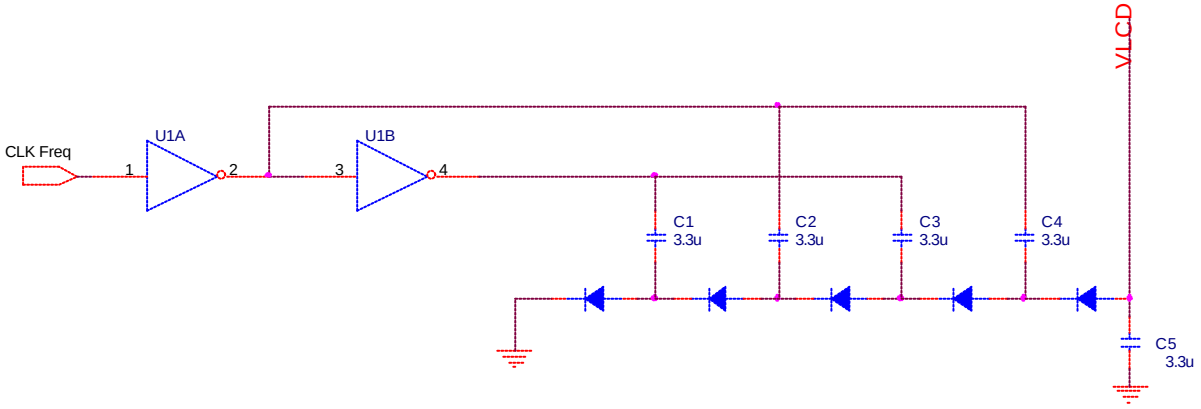
Data flow direction: The LCD display segment data direction is S160 to S01

Reference of DC booster for Vlcd

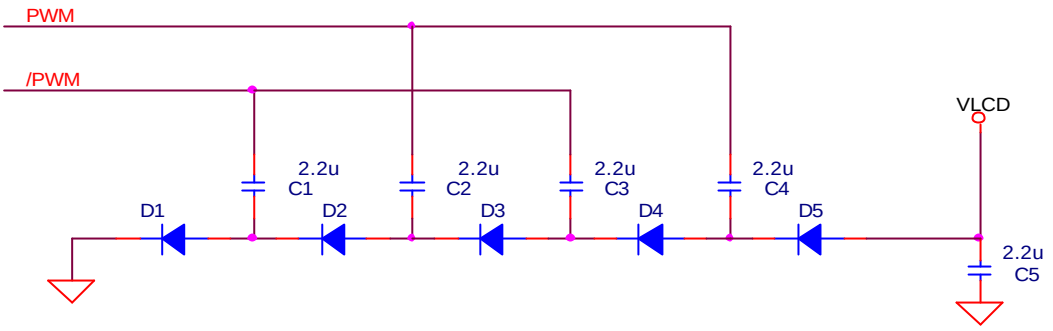
1. Use external oscillator for booster



2. Use MPU signal to generate clock pulse for booster



3. Use PWM output of MCU for booster



*Note:

Diode recommends using BAT54 or Schottky diode.

Inverter for buffer for CLR pulse. If MPU CLK output can drive more than 1mA current, then inverter may be omitted.

Increase value of capacitor will give higher drive for booster circuit.

The circuit within dotted line is for controlling the contrast of LCD. Set higher duty ratio for dimmer LCD, lower duty ratio for darker LCD.

Revisions:

Version 1

First release

Version 2

Page All	Change name of Pad	V1 → V5 V2 → V0 V4 → V2
Page 9	Application circuit (2) update	

Version 3

Page 11	Change value of capacitors, add contrast control.

Version 4

Page 3,4	Update for pad diagram and pad coordinates.

Version 5

Page 11	Add the PWM booster circuit.

Version 6

Modify datasheet cover