Alphanumeric
Liquid crystal display (LCD) controller

SA3070B

Technical Specification

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1. Description

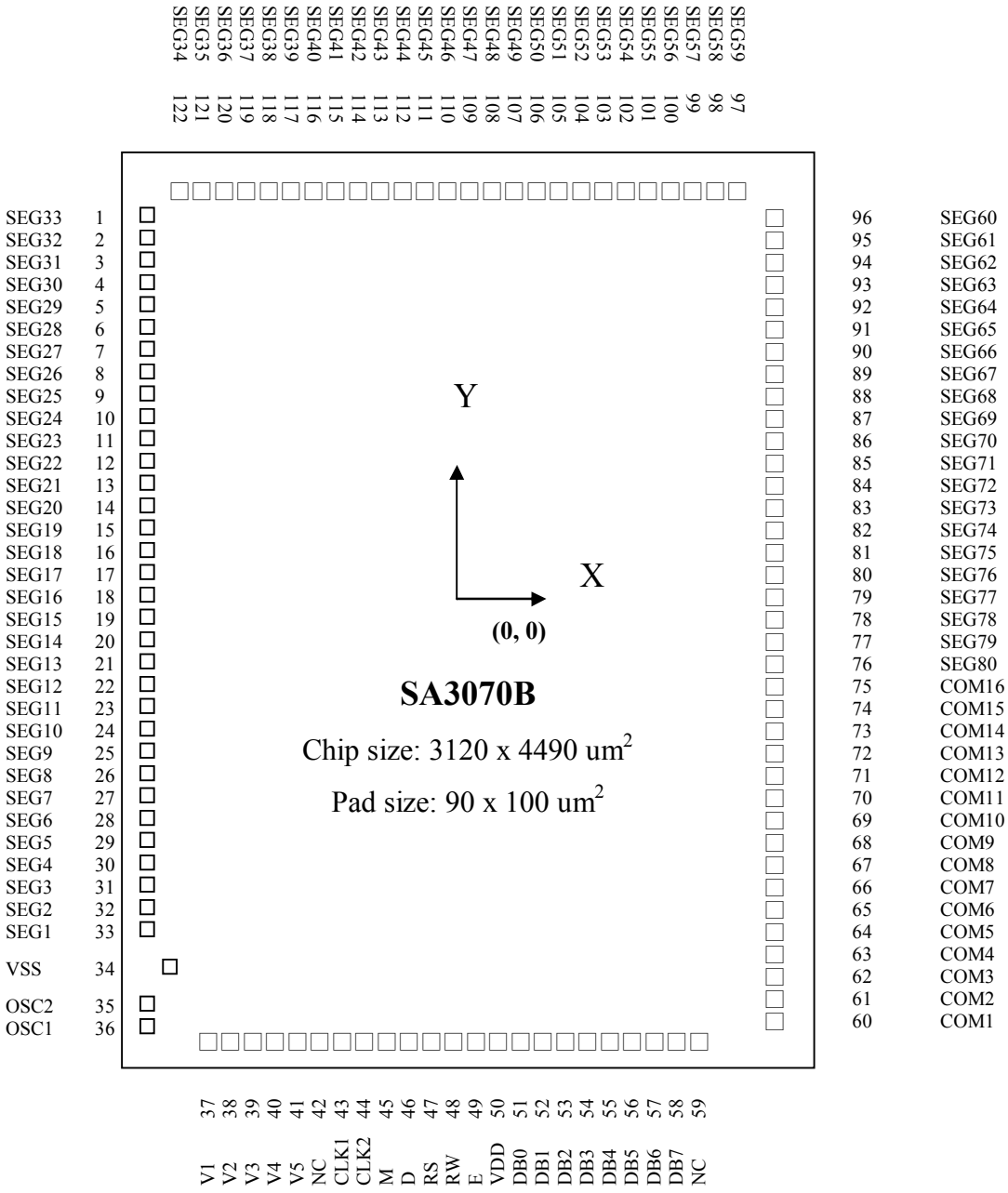
1.1 Features

- Built-in Bias Resistors = 4K Ohm±15%
- Internal memory
  - Character Generator ROM
  - Character Generator RAM: 320 bits
  - Display Data RAM: 80 x 8 bits for 80 digits
- Power Supply Voltage: 2.7 ~ 5.5V
- Compatible and extended modes for flexible application
- LCD Supply Voltage 3 ~ 10V (VDD-V5)
- CMOS Process
- 1/8 duty, 1/11 duty or 1/16 duty selectable
  - 1/8 duty, 5x7 dots formal 1 line,
  - 1/11 duty, 5x 10 dots formal 1 line, or
  - 1/16 duty 5x7 formal 2 line
- Bare Chip Available

1.2 Applications

- Character type dot matrix LCD driver and controller.
- Internal driver: 16 common and 80 segment signal output.
- Display character format: 5x7 dots + cursor, 5 x 10 dots + cursor
- Easy interface with 4 or 8 bits MPU
- Display character pattern: refer to font table
- The special character pattern can be programmable by Character Generator RAM directly.
- Automatic power on reset function
- It is possible to read both Character Generator RAM and Display Data RAM from MPU.

1.3 Pad diagram



Substrate should be connected VDD or floating and use 1 mil bonding wire

1.4 Pad Coordinates

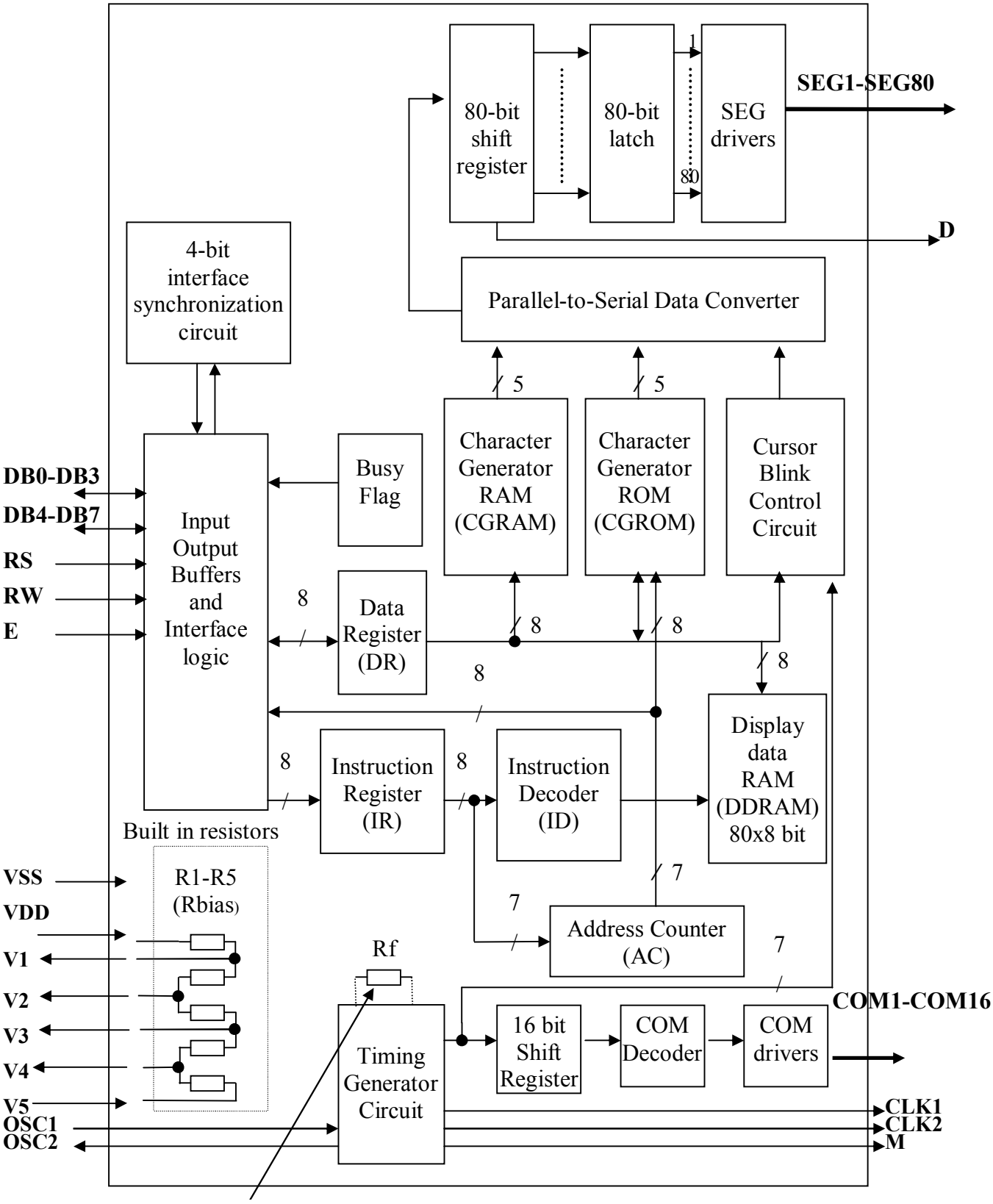
Pad No	Pad Name	Coordinates	
		X (μm)	Y (μm)
1	SEG33	-1428.7	1904.1
2	SEG32	-1428.7	1794.1
3	SEG31	-1428.7	1684.1
4	SEG30	-1428.7	1574.1
5	SEG29	-1428.7	1464.1
6	SEG28	-1428.7	1354.1
7	SEG27	-1428.7	1244.1
8	SEG26	-1428.7	1134.1
9	SEG25	-1428.7	1024.1
10	SEG24	-1428.7	914.1
11	SEG23	-1428.7	804.1
12	SEG22	-1428.7	694.1
13	SEG21	-1428.7	584.1
14	SEG20	-1428.7	474.1
15	SEG19	-1428.7	364.1
16	SEG18	-1428.7	254.1
17	SEG17	-1428.7	144.1
18	SEG16	-1428.7	34.1
19	SEG15	-1428.7	-75.9
20	SEG14	-1428.7	-185.9
21	SEG13	-1428.7	-295.9
22	SEG12	-1428.7	-405.9
23	SEG11	-1428.7	-515.9
24	SEG10	-1428.7	-625.9
25	SEG9	-1428.7	-735.9
26	SEG8	-1428.7	-845.9
27	SEG7	-1428.7	-955.9
28	SEG6	-1428.7	-1065.9
29	SEG5	-1428.7	-1175.9
30	SEG4	-1428.7	-1285.9
31	SEG3	-1428.7	-1395.9
32	SEG2	-1428.7	-1505.9
33	SEG1	-1428.7	-1615.9
34	VSS	-1394.1	-1775.9
35	OSC2	-1428.7	-1973.8
36	OSC1	-1428.7	-2088.1
37	V1	-1277.3	-2113.7
38	V2	-1167.3	-2113.7
39	V3	-1057.3	-2113.7
40	V4	-947.3	-2113.7
41	V5	-837.3	-2113.7
42	NC	-727.3	-2113.7
43	CLK1	-586.3	-2113.7
44	CLK2	-476.3	-2113.7
45	M	-366.3	-2113.7
46	D	-256.3	-2113.7
47	RS	-146.3	-2113.7
48	RW	-36.3	-2113.7
49	E	73.7	-2113.7
50	VDD	183.7	-2113.7
51	DB0	293.7	-2113.7
52	DB1	403.7	-2113.7
53	DB2	513.7	-2113.7
54	DB3	623.7	-2113.7
55	DB4	733.7	-2113.7
56	DB5	843.7	-2113.7
57	DB6	953.7	-2113.7
58	DB7	1063.7	-2113.7
59	NC	1173.7	-2113.7
60	COM1	1428.7	-2065.9
61	COM2	1428.7	-1945.9

Pad No	Pad Name	Coordinates	
		X (μm)	Y (μm)
62	COM3	1428.7	-1835.9
63	COM4	1428.7	-1725.9
64	COM5	1428.7	-1615.9
65	COM6	1428.7	-1505.9
66	COM7	1428.7	-1395.9
67	COM8	1428.7	-1285.9
68	COM9	1428.7	-1175.9
69	COM10	1428.7	-1065.9
70	COM11	1428.7	-955.9
71	COM12	1428.7	-845.9
72	COM13	1428.7	-735.9
73	COM14	1428.7	-625.9
74	COM15	1428.7	-515.9
75	COM16	1428.7	-405.9
76	SEG80	1428.7	-295.9
77	SEG79	1428.7	-185.9
78	SEG78	1428.7	-75.9
79	SEG77	1428.7	34.1
80	SEG76	1428.7	144.1
81	SEG75	1428.7	254.1
82	SEG74	1428.7	364.1
83	SEG73	1428.7	474.1
84	SEG72	1428.7	584.1
85	SEG71	1428.7	694.1
86	SEG70	1428.7	804.1
87	SEG69	1428.7	914.1
88	SEG68	1428.7	1024.1
89	SEG67	1428.7	1134.1
90	SEG66	1428.7	1244.1
91	SEG65	1428.7	1354.1
92	SEG64	1428.7	1464.1
93	SEG63	1428.7	1574.1
94	SEG62	1428.7	1684.1
95	SEG61	1428.7	1794.1
96	SEG60	1428.7	1904.1
97	SEG59	1396.3	2114.5
98	SEG58	1276.3	2114.5
99	SEG57	1156.3	2114.5
100	SEG56	1046.3	2114.5
101	SEG55	936.3	2114.5
102	SEG54	826.3	2114.5
103	SEG53	716.3	2114.5
104	SEG52	606.3	2114.5
105	SEG51	496.3	2114.5
106	SEG50	386.3	2114.5
107	SEG49	276.3	2114.5
108	SEG48	166.3	2114.5
109	SEG47	56.3	2114.5
110	SEG46	-53.7	2114.5
111	SEG45	-163.7	2114.5
112	SEG44	-273.7	2114.5
113	SEG43	-383.7	2114.5
114	SEG42	-493.7	2114.5
115	SEG41	-603.7	2114.5
116	SEG40	-713.7	2114.5
117	SEG39	-823.7	2114.5
118	SEG38	-933.7	2114.5
119	SEG37	-1043.7	2114.5
120	SEG36	-1153.7	2114.5
121	SEG35	-1273.7	2114.5
122	SEG34	-1393.7	2114.5

1.5 Pin Description

Pin Name	Input/Output	Function	Interface
VDD	-	Positive voltage for logic circuit and LCD drivers	Power supply
VSS	-	Ground (0V)	Power supply
V5	-	Bias voltage level for LCD driving	Power supply
V1, V2, V3, V4	-	Bias voltage level for LCD driving **Divided by five built-in resistors (1/5 bias)(*built-in resistors type)** $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$. V5 – GND or other voltage	Power supply
COM1 - COM16	Output	Common signal outputs for LCD	LCD
SEG1 - SEG80	Output	Segment (information) outputs for LCD	
OSC1, OSC2	Input (OSC1), Output (OSC2)	When use internal oscillator, connect the external Rf resistor. If external clock is used, connect it to OSC1 (no built-in resistors type) **Bonding or not for adjusting OSC frequency at VDD = 5V or 3V (*built-in resistors type)**	External resistor/Oscillator(OSC1)/ **no connection**
CLK1, CLK2	Output	Each outputs extension driver latch clock and extension driver shift clock	Extension driver
D	Output	Output of the serial data for the extension drivers	
M	Output	The alternating signal to change voltage polarity between outputs COM and SEG.	
RS	Input (Pull-up to VDD)	Signal for selection of an interface register. At RS=1 the data register is selected for the reading and writing. At RS=0 an instruction register is selected (when writing) or the flag busy condition and a current address (when reading).	MPU
RW	Input (Pull-up to VDD)	Selection of the reading/writing mode. When RW=1 – reading operation, When RW=0 – writing operation.	
E	Input	MPU enable signal	
DB0 - DB3	Inputs/Output (Pull-up to VDD)	Lower 4 bit data of the MPU bi-directional interface in 8-bit mode. Not used in 4-bit mode.	
DB4 - DB7	Inputs/outputs (Pull-up to VDD)	Higher 4 bit data of the MPU bi-directional interface in 8-bit mode. In 4-bit interface mode used for the serial transfer of the high order and low order data. DB7 used for the reading of the flag busy condition.	
NC	No connection	This pins must be fixed to open	

1.6 Block Diagram



*Built-in resistors type

Figure 1. SA3070B block diagram

2. Logic control sub-system

2.1. MPU interface

Interface registers

The SA3070B controller has two interface registers: instruction register (IR) and data register (DR). An instruction register – is write only and accepts an instruction code from the data bus. The data register is both read and write. (input – DRin and output DRout). The data exchange between the registers and MPU is performed through bi-directional Data Bus (DB) of MPU interface.
The registers are selected by RS (Register Selector) signal and read/write operations are implemented by RW (Read-Write) signal according to table 1.

The IR register is used for an instruction code store while instruction executing. The DRin register is used for the temporary storage of data to be information write to DDRAM or CGRAM.

Table 1 Registers interface selection

RS	RW	Operation
0	0	Instruction writing into IR
0	1	Reading of Busy Flag (DB7) and Address Counter (DB6-DB0)
1	0	Data writing into DR
1	1	Data reading from DR

While executing any instruction RAM (DDRAM or CGRAM) data always is read automatically and the DRout output register always contains data from the last address (even if the address was changed during instruction execution). During the next read instruction implementation these data can be read through MPU interface. Thus it is guaranteed that MPU always will receive data from the last address.

The general destination of the interface registers is the separation of the MPU interface-timing diagram from an internal controller-timing diagram. The controller operation is realized according to an internal timing diagram, which is clocked by the sufficiently low frequency of the clock generator. The IR and DR registers allow rapidly the data to write and read, released the MPU data bus during the instruction execution.

An instruction is executed on the falling edge of the E signal. On the DB [7:0], RS, RW inputs of an improved interface are installed the additional internal delays according to E signal with duration of not less 40 ns. It is allow to install all interface signals simultaneously by single MPU instruction, if the signals delays and edges on the interface bus not exceed 40 ns.
During the execution of an instruction, the register state is locked and the content in the register cannot be changed.

Busy Flag (BF)

Before writing the next instruction, MPU must ensure that previous instruction is completed and interface registers are free. To do this, MPU can check the Busy Flag (BF). If Busy Flag = 1, the controller is executing the previous instruction and MPU must perform idle cycles or other operations to wait for the busy flag to go to 0 state.

Busy Flag is read when RS=0 and RW=1 at DB7 output (see Table 1). The BF read procedure and current address is used only to check the controller current state and is not an instruction, therefore it does not lock input registers.

4-and 8-bit interface

SA3070B controller can operate with 4- or 8- bit data bus interface with MPU. The 4-bit, 8-bit interface choice is made by "Functional state setting" instruction.

- In 8-bit mode of the bit interface all 8 bits of the data bus are used. The data are strobe by the falling edge of E signal. On the falling edge of the E signal an instruction execution is started and Busy Flag (BF) is set to "1" (see Figure 2).
- In the 4-bit interface mode, DB4-DB7 is used for information exchange with MPU. DB0-DB3 bits are not used. The 8-bit instructions and data are transmitted through the 4-bit interface in two passes. Accordingly two E pulses are needed (see Figure.3). Firstly 4 high order bits are transferred and then 4 low order bits. An internal controller data selector multiplexes the high or low tetrad of this register, switching on E signal falling edge. The instruction is completed on the second E pulse and accordingly Busy Flag is set to "1" only on falling edge of second E pulse.

  Each instruction should be accompanied strictly by two E pulses. If this condition is violated, the sequence of data will be broken; thereof the high and low data tetrads in the controller registers exchange their places. Missing any one of the two E pulses, owing to MPU synchronization loss or noise influence will break all further functioning of the controller, since the instructions transfer is disrupted, the processor can be lose Busy Flag and so on.

  To prevent this situation, the controller has the interface synchronization function, which provide the correct order of the data following in 4-bit interface: any change of both RS as well as RW signals reset the data selector to the initial state (see Figure 3). In other words the any change of the interface operation mode (even Busy Flag check) automatically set it in initial state. On the other hand, it is forbidden to change RS and RW state between E pulses during submission of single instruction.

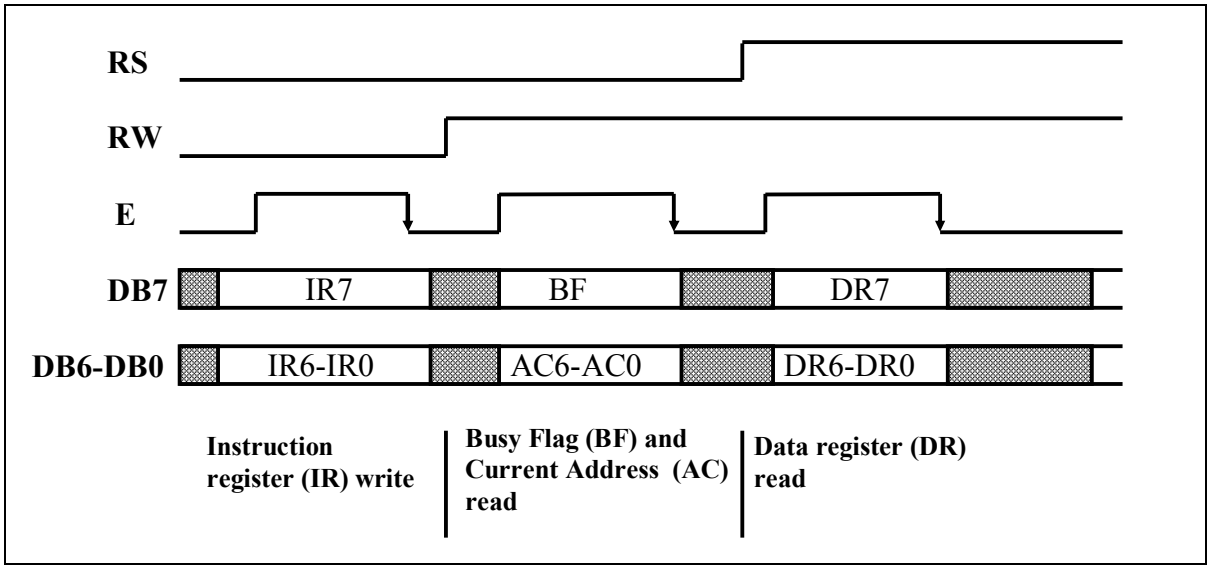


Figure 2. Example of 8-bit interface operation.

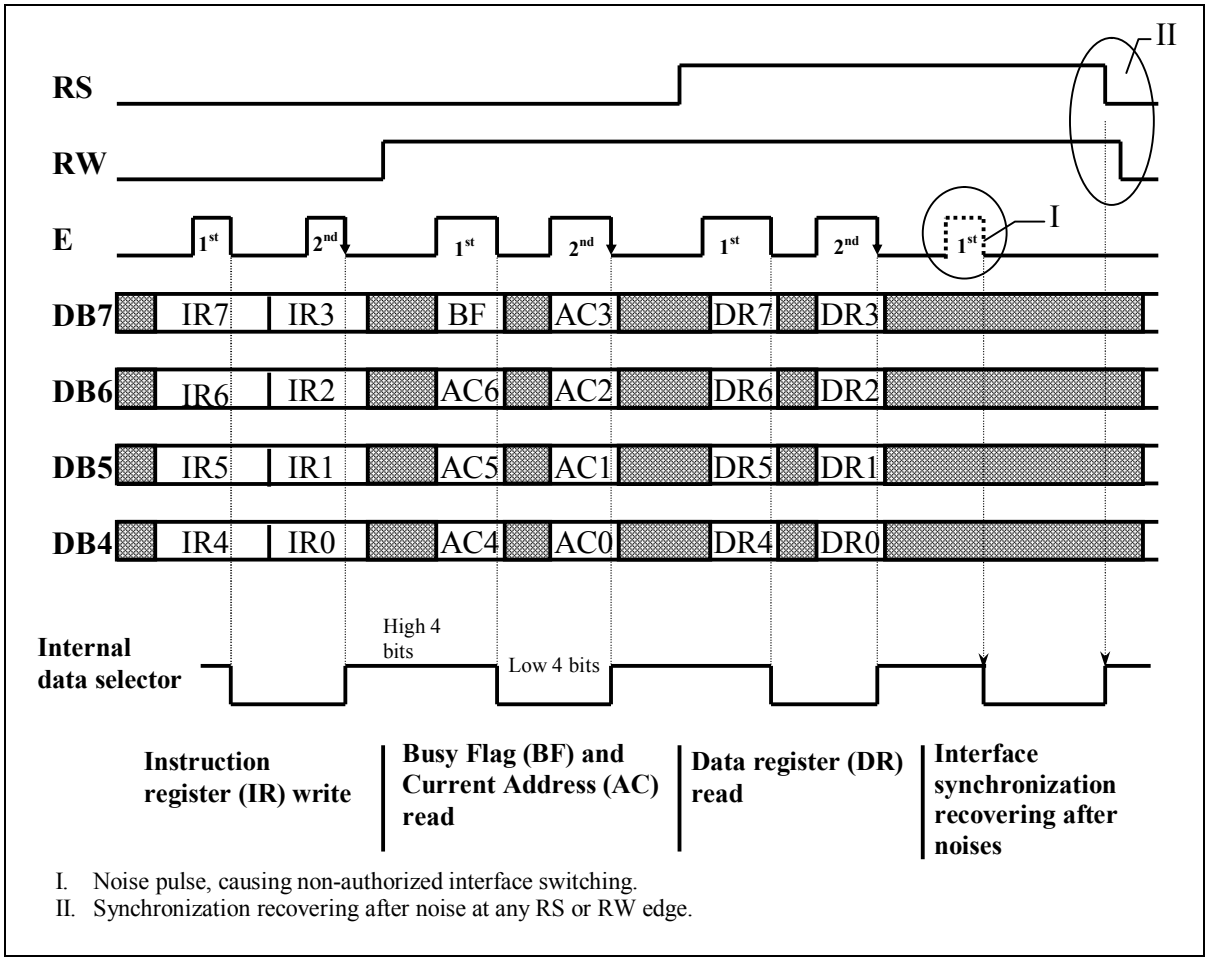


Figure 3. Example of 4-bit interface operation.

2.2. DDRAM address distribution

The controller can display characters in one or two lines. The suitable mode is set by "Functional state set" instruction.

In one-line mode the controller display the 5x8 or 5x11 characters in single DDRAM addresses range from 0 up to 79 (4Fh). COM [1...8] lines are used for 5x8 characters or COM [1...11] lines are used for 5x11 characters.

In two-line mode the controller display the 5x8 characters in two lines accordingly:

- DDRAM addresses range from 0 up to 39 (27h) for the first line (COM [1...8]),
- DDRAM addresses range from 64 (40h) up to 103 (67h) for the second line (COM [9...16]).

In the display mode of the 10x15 large characters for theirs are used the COM [2...16] lines and DDRAM addresses from 0 up to 39. For the display of the icons line is used COM1line and DDRAM addresses from 64 up to 103.

The correspondence between DDRAM addresses and the character positions on display in one-line mode and also an example of cursor displaying in current display position, are shown in Figure 4.The correspondence between DDRAM addresses and the character positions on display in two-line mode and also an example of cursor displaying in current display position, are shown in Figure 6.The correspondence between DDRAM addresses and the characters positions on display in the large characters, are shown in Figure 8.

2.3. Current address counter

The current address, on which is implemented an access to the memory (DDRAM and CGRAM), and also determined the cursor position on display, are determined by Current Address Counter (AC). The counter has the functions of clearing in 0 state, setting of specified state, incrementing and decrementing.

AC reset to 0 is realized by "Display Clear" and "Home Return" instructions.

The set of AC random address is implemented by "Address DDRAM Set" and "Address CGRAM Set" instructions. In this case the new address is written in AC from Instruction register (IR). By these instructions is also determined the memory type, to which are realized all following accesses.

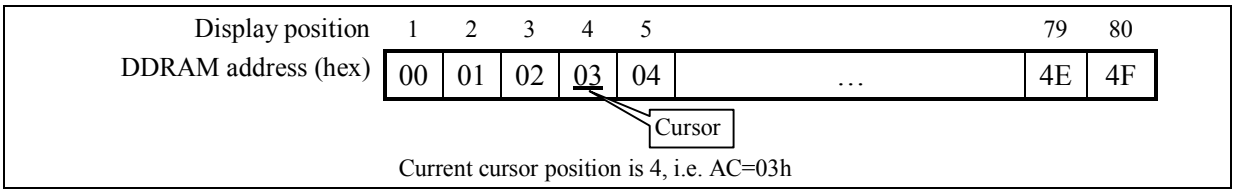


Figure 4. One-line display without shift.

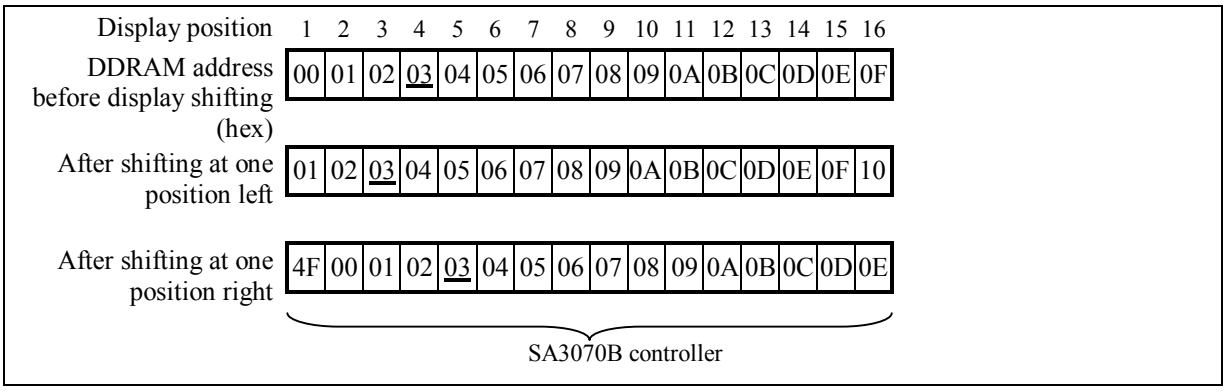


Figure 5. Display shift in one-line mode.

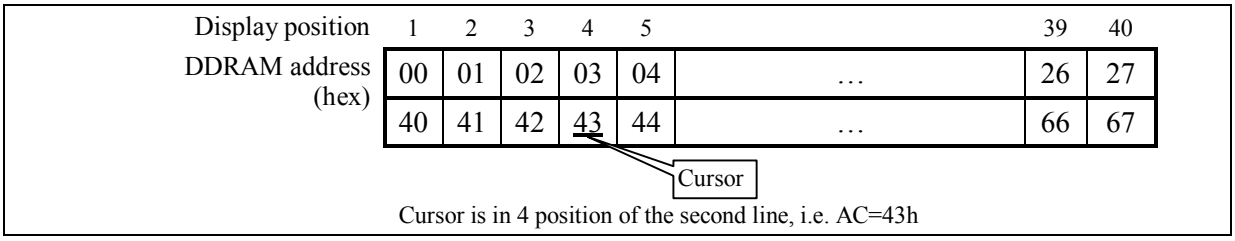


Figure 6. 2-lines display without shift.

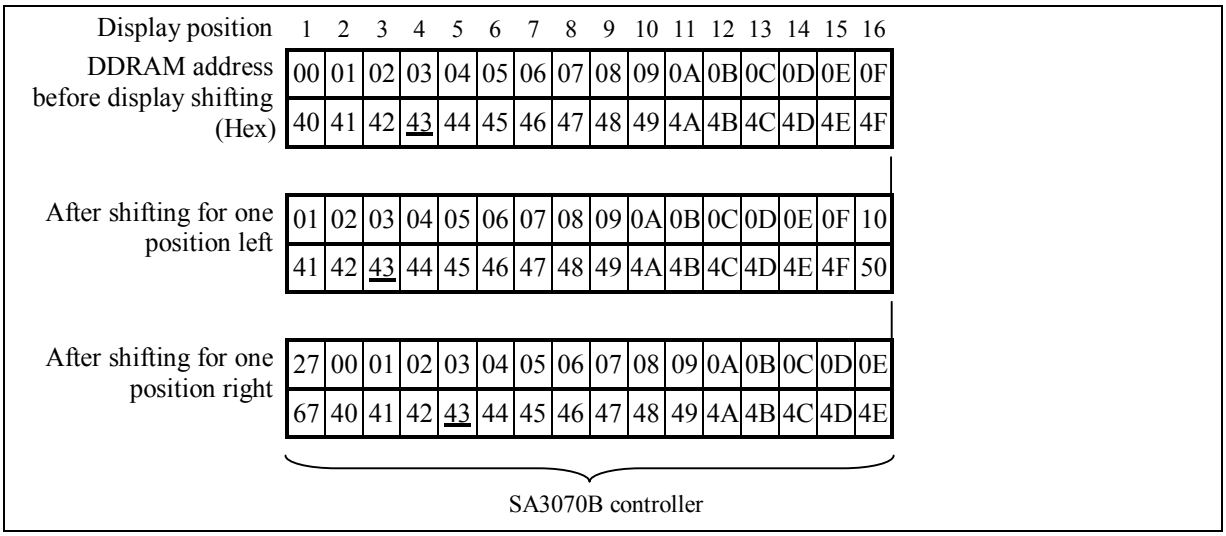


Figure 7. Display shift in 2-line mode.

2.4. Refresh Start Address Counter and display shifting

The Start Address Counter is used for the display shifting. The state of this counter indicates the DDRAM address, used in the beginning of COM each line sweep (sweep display line) in each cycle of the Screen Refresh. The counter has a reset function and the incrementing/decrementing functions.

The counter reset to the initial state by "Display Clear" and "Home return". After this an information on the display is displayed from 0 address of DDRAM.

The counter incrementing or decrementing is realized by "Display Shift" instruction with an indication of the shift direction. The count order is the same as for the AC counter for DDRAM address.

The counter has no the random address set function, and its state is not readable through MPU interface.

The correspondence between the DDRAM addresses and the displayed characters positions after left/right display shift in 1-line mode is shown in Figure 5.

The correspondence between the DDRAM addresses and the displayed characters positions after left/right display shift in 2-line mode is shown in Figure 7.

The correspondence between the DDRAM addresses and the displayed characters positions after left/right display shift in the large characters mode is shown in Figure 9.

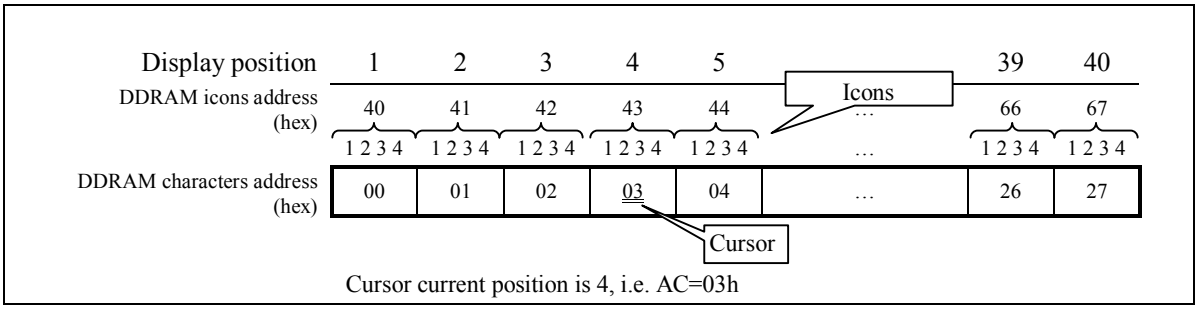


Figure 8. Display without shift of the driver.

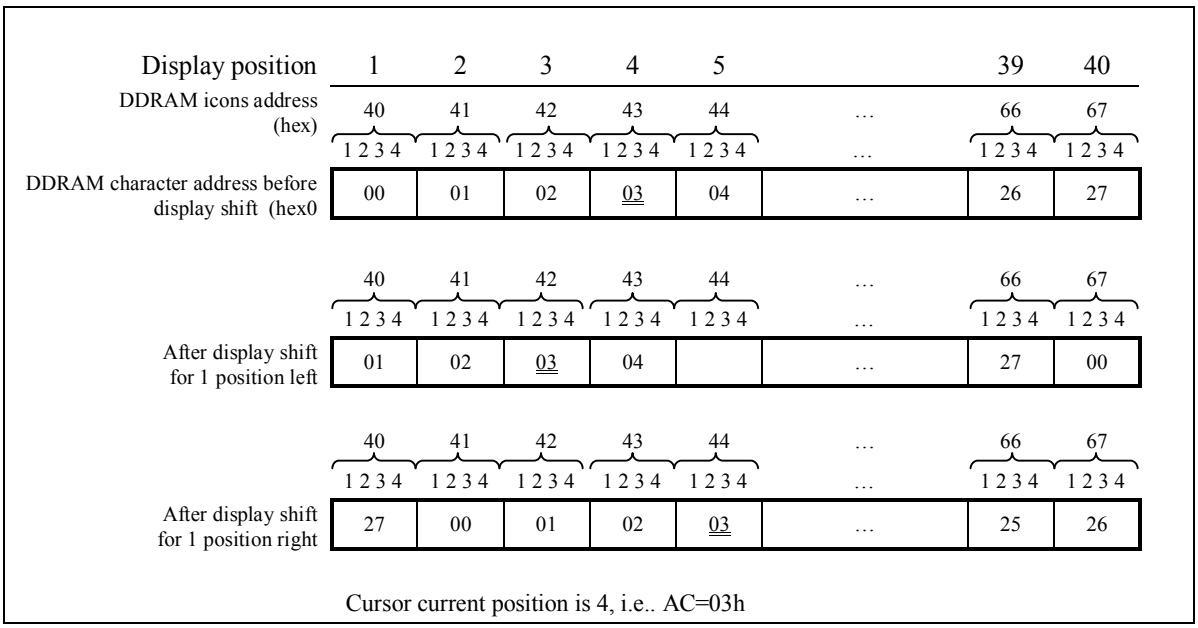


Figure 9. Display shift of the driver.

2.5. Controller timing diagram forming

The internal controller-timing diagram consists from elemental cycles by 5 clocks length. This is the time for an data output for one character to an output SEG shift register, as the characters width - 5 bit and an each bit occupy 1 clock.

An each elemental cycle consists from the controller-timing diagram three phases, which continuously cyclically follow one after another:

1) Phase of data writing to DDRAM/CGRAM and instructions execution,
2) Phase of data reading from DDRAM/CGRAM to output data register of MPU interface,
3) Phase of data reading from DDRAM/CGRAM/CGROM and the characters displaying on the LCD screen (i.e. screen refresh phase).

This solution provides the complete time division between competitive memory access processes for the implementation of the MPU instructions and the information refresh on the LCD screen. The MPU interface operates only with the IR and DR interface registers independently from the controller internal timing diagram and on the own frequency, determined by MPU. The single condition for the MPU interface, determined by an internal state of controller, - the wait of the current instruction execution completion according to the Busy Flag state.

Phase 1 (2 clocks) provides the MPU instructions execution, including the instructions, connecting with controller memory accessing. The memory accessing occur on the address, installed in AC. If is necessary, after the data writing phase completion the data address is incremented or decremented.

Phase 2 (1 clock) destine for the data reading from DDRAM / CGRAM to output data register. Since the reading phase follows the writing and instruction execution, data are read after an address changing (that is on the new address), if it took place during an instruction execution. The following the data reading instruction will allow to bring out this data on the MPU interface, and the data register will be filled with new data from the next memory address.

Phase 3 (2 clocks) connected with the information refresh on the LCD screen and destined for the data transferring from CGRAM / CGROM to the data shift register. At the same time as CGRAM / CGROM address are used the character code, written in DDRAM, the bank numbers and CGROM pages, and also the current active COM number.

For any instruction execution (except "Display Clear") the obligatory complete pass of the 1st and 2nd phases of the timing diagram, together these two phases constitute the Instruction execution phase with the duration of 3 clocks. Therefore, the instruction execution time can be from 3 up to 8 clocks. The "Display Clear" instruction implement the serial writing of the space code (20h) in all 80 cells of DDRAM, that takes not more than 403.5 clocks.

There is possibility of the rapid instructions execution under some additional conditions.

The timing diagram of the LCD screen sweep depends from the displaying information mode.

In 1-line mode on each COM display 80 characters, on 5 bit on each character, therefore the active COM duration in this mode is 80x5=400 clocks (1.48ms at fosc=270kHz). The screen refresh period in this mode is:

- For 5x8 font (i.e.. 8 active COM lines): 8x1.48=11.84ms, i.e. frame frequency is ~84.3Hz.
- For 5x11 font (i.e. 11 active COM lines): 11x1.48=16.28ms, i.e. frame frequency is ~61.4Hz.

In 2-line mode on each COM is display 40 characters, for that is required 40x5=200 clocks. (0.74ms at fosc=270kHz). The screen refresh period is 16x0.74=11.84ms, i.e. frame frequency is ~84.3Hz.

2.6. Character and cursor blinking

For the character or cursor blinking function realization the frequency timer-divider, driving the blinking period ≈0.76 s at the oscillator frequency fosc=270kHz, is used. The blinking cursor or character is placed in the position, driven by the AC address counter.

2.7. Issuing and execution of instructions

The SA3070B controller has only two program accessible registers: the instruction register (IR) and the data register (DR). The number of this registers states and also the control signals (RW – Read/Write and RS – Register Select) determine the controller instruction set (Table 5). It is possible conditionally the all instruction set to divide on 4 categories:

- Determination of the controller operation mode (display format, interface bit capacity, cursor displaying and character blinking mode etc.);
- Setting of the RAM internal address and of the cursor current position (setting of DDRAM/CGRAM address, cursor shift);
- Data transferring between internal RAM and MPU;
- Service functions executing (Display Clear, Reset, Display Shift etc).

Usually the most of executing instructions are the data transferring in memory instructions. For the simplification and speed-up the memory loading the controller has auto incrementing function (or auto decrementing) of RAM address.

For the correct controller functioning before each instruction writing must ensure that the previous instruction is completed. This can be made by two ways:

- Busy Flag (BF) check, until it set in 0 state. It's the most efficient way (see Figures 10 & 11).
- With the time delay before the following instruction issuing, exceeding the maximal time of the previous instruction implementation (see Table 5). It's a more simple and slow method, but it is usable when the data reading mode from the controller is never used (on the RW output is fixed log.0 state). The synchronization function of the 4-bit interface allow to control by controller providing the maximal reliability level at the using only 6 interface signals (DB [7:4], E, RS).

The instructions execution time is decreased in the large characters mode at the clock frequency increasing. All instructions, excepts "Display Clear", are executed during not more 8 clocks, for frequency Fosc=500kHz – this is 8x2µs=16µs.

The "Display Clear" is implemented not more 203.5 clocks, i.e. 203x2µs=506µs.

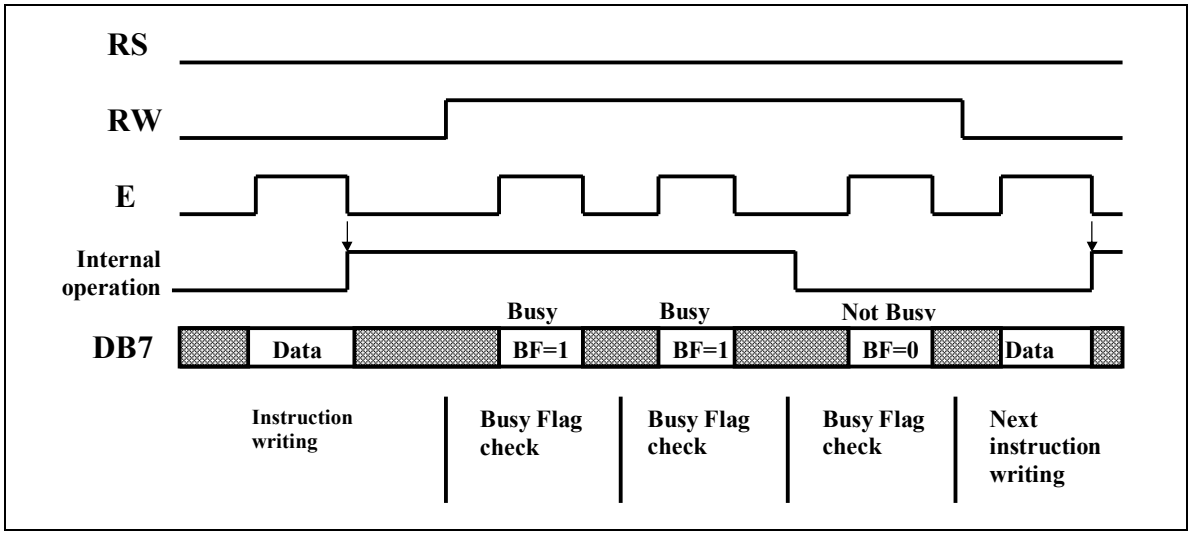


Figure 10. Example of instruction issuing with Busy Flag check in 8-bit interface mode.

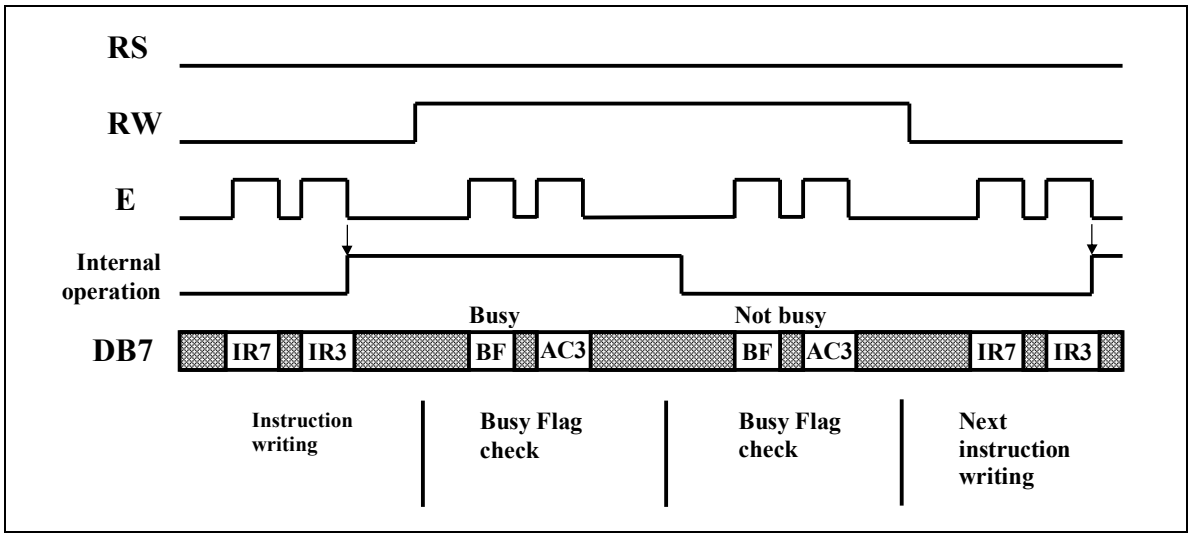


Figure 11. Example of instruction issuing with Busy Flag check in 4-bit interface mode.

Table 5. Instructions set of SA3070B controller

Instruction	Instruction code										Description	Maximum exec. time (fosc=270 kHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	**1**	Clear of an entire display contents and set of the address counter (AC) and the display shift counter in 0 state. In large characters mode only clear of character line.	1.53ms
Home return	0	0	0	0	0	0	0	0	**1**	-	Set of AC and Display shift counter 0 state. DDRAM contents unchanged	1.53ms
Input Mode Set	0	0	0	0	0	0	0	**1**	**I/D**	**S**	Set of cursor shift direction at the data writing or data reading in DDRAM and the display shift enable (only for writing)	39µs
Display on/off	0	0	0	0	0	0	**1**	**D**	**C**	**B**	On/off control of entire display (D), cursor (C), or character or cursor blinking (B)	39µs
Display or cursor shift	0	0	0	0	0	**1**	**S/C**	**R/L**	–	–	Display or cursor shift to right (S/C) or to left (R/L)	39µs
Functional set	0	0	0	0	**1**	**DL**	**N**	**F**	–	–	Set of interface data length (DL), display line number (N), character font (F), current bank number	39µs
CGRAM address set	0	0	0	**1**	**AC5**	**AC4**	**AC3**	**AC2**	**AC1**	**AC0**	CGRAM 6-bit address set. After set of this instruction the data are written and read in/from CGRAM.	39µs
DDRAM address set	0	0	**1**	**AC6**	**AC5**	**AC4**	**AC3**	**AC2**	**AC1**	**AC0**	DDRAM 7-bit address set. After set of this instruction the data are written and read in/from DDRAM.	39µs
Busy Flag and current address reading	0	**1**	**BF**	**AC6**	**AC5**	**AC4**	**AC3**	**AC2**	**AC1**	**AC0**	Busy Flag and also current address counter (AC) state reading, denotative the current instruction implementation	0µs
Data write in CGRAM or DDRAM	**1**	**0**	**Written data**								Data write in CGRAM or DDRAM	43µs
Data read from CGRAM or DDRAM	**1**	**1**	**Readable data**								Data read from CGRAM or DDRAM	43µs

I/D: 1-incrementing, 0- decrementing
S: 1- display shift enable when write to DDRAM
D: 1- display is on, 0- display is off
C: 1- cursor is on, 0- cursor is off
B: 1- blinking is on, 0- blinking is off
S/C: 1- display shift, 0- cursor shift
R/L: 1- shift to the right, 0- shift to the left
DL: 1- 8-bit interface, 0- 4-bit interface
N: 1- two-line display, 0- one-line display
F: 1- 5x11 font, 0- 5x8 font

DDRAM –Displaying data RAM contents the characters, displaying on the screen, codes.
CGRAM –Character Generator RAM contents the characters, determined by user.
A_{CG} – CGRAM 6-bit address.
A_{DD} – DDRAM 7-bit address.
AC – Address Counter for CGRAM, and DDRAM addressing.
BF: 1- instruction execution, 0- instruction setting enable
– have no significance

2.8. Instructions description

Display Clear

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

The "Display Clear" instruction writes 20h code into all DDRAM addresses (in CGROM coding that must be the space code). Then an address counter (AC) and display shift counter are set in 0 state. In other words, an initialisation of the display data and the display and cursor state take place. It also set the I/D bit of "data input mode" to "1" state, the S bit state does not change.

In large characters mode an instruction clear only the characters line on the DDRAM 0-27h (39) addresses. The icons line state on the 40h-67h (64-103) addresses does not change.

Reset

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

The "Reset" instruction set AC address in 0, and also returns the display to its initial state, if it was shifted. The DDRAM contents do not change. The I/D bit of the "Data input mode" instruction set in "1", the S bit state do not change.

According to there settings the cursor returns in the first position of screen (in the first line, if display is in the two-line mode).

Data input mode set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	ID	S

I/D: incrementing (ID=1) or decrementing (ID=0) of the Address Counter (AC) when the data writing or reading in DDRAM or CGRAM. Accordingly, the cursor and the character blinking are shifted to the right at an incrementing and to the left at the decrementing.

S: Display shift enable to the left (ID=1) or to the right (ID=0) at S=1 during writing of the character code to DDRAM. At S=0 display shift is disabled. At an accessing to CGRAM the display shift is not occur and this bit state have not the significance.

When the display shift is enabled, it is occur simultaneously with the cursor shift, but it direction is in opposition to the cursor move direction. Thus, an effect is created, the cursor stay on the place, and entire display along with the setting character is moved in opposite direction.

Display on/off

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

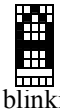
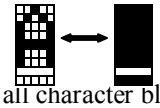
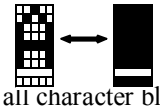
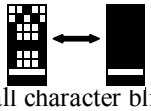
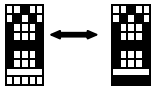
D: The display is on when D=1 and off when D=0. At that, all written data are stored in memory, but at D=0 theirs are not displayed. The cursor and character blinking also are not displayed.

The constant accessing to the memory, connected with the screen refresh, is absent. When the storing mode is enabled (determined by the mask option), at the display switching off is occur the transition in this mode with the switching off the internal or external resistive divider V_{LCD} for saving of the consumed power (see part. 2.11).

C: At C=0 the cursor off, at C=1 the cursor is on and displayed on the screen in position, corresponding to the AC.

B: Switch on (B=1) and switch off (B=0) of the character and the cursor blinking.

Table6. Cursor displaying and character blinking modes

C	B	Cursor blinking disable	Cursor blinking enable
0	0	 Cursor is off, blinking is off	 Cursor is off, blinking is off
0	1	 Cursor is off, all character blink	 Cursor is off, all character blink
1	0	 Cursor is on, blinking is off	 Cursor always on, blinking is off
1	1	 Cursor is on, all character blink	 Cursor blink

Cursor and Display Shift

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

This instruction shift cursor or entire display to the left or to the right without changing of the memory contents (see Table 7). The cursor shift is represent the incrementing or the decrementing of the address counter (AC). The shift of an entire display represent the incrementing or the decrementing of the initial address counter at the screen refresh without changing of the AC state, as a result the cursor follow behind the display shift.

At the cursor shift in the two-line mode the cursor is moved from first line into second line and conversely according to the regulations of address count (AC)

At the display shift in two-line mode the characters in each line are shifted parallel and not pass from one line in another (see Figure 7).

Table 7. Cursor and Display Shift modes

S/C	R/L	Description
0	0	Cursor shift to the left (AC is decremented by 1)
0	1	Cursor shift to the right (AC is incremented by 1)
1	0	Display shift to the left (start refresh address is incremented by 1)
1	1	Display shift to the right (start refresh address is decremented by 1)

Functional state set

The instruction is destined for the setting of the controller basic operation parameters setting. The destination of the bit instruction depend from the characters displaying mode on the screen.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

Table 8. Functional state instruction set

N	F	Display lines number	Font size	Multiplexing level	Notes
0	0	1	5x8	1/8	
0	1	1	5x11	1/11	
1	x	2	5x8	1/16	Displaying of 2 lines of 5x11 characters is impossible

x – have not a significance

CGRAM address set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC[5]	AC[4]	AC[3]	AC[2]	AC[1]	AC[0]
				MSB					**LSB**

The CGRAM address set instruction write CGRAM 6-bit address in the address counter (AC). It is simultaneously set the CGRAM access flag, as a result the following data write/read instructions will to direct theirs in CGRAM.

DDRAM address set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC[6]	AC[5]	AC[4]	AC[3]	AC[2]	AC[1]	AC[0]
			MSB						**LSB**

The DDRAM address set instruction write the DDRAM 7-bit address in the address counter (AC). It is simultaneously set the CGRAM access flag, as a result the following data write/read instructions will to direct theirs in DDRAM.

In the one-line display (N=0) for the DDRAM access the AC [6..0] address must to be in 00h-4Fh (0-79) range. In the two-lines display (N=1) for the DDRAM access the AC [6..0] address must to be in 00h-27h (0-39) range for first line and in 40h-67h (64-103) range for second line. In the large characters mode the AC [6..0] address must to be in 00h-27h (0-39) range for the character line and in 40h-67h (64-103) range for icons.

The controller version and the operation mode identifier is placed in DDRAM 78h-7Fh addresses range (120-127, see part 3.4).

Busy Flag and Current Address Read

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC[6]	AC[5]	AC[4]	AC[3]	AC[2]	AC[1]	AC[0]
			MSB						**LSB**

The read procedure of Busy Flag (BF) and AC current address allow to determine the controller busy state during an execution of the current instruction. If BF=1, the controller is in the state of the instruction execution, therefore, the new instruction, given in this moment, will ignored. For the correct input of the next instruction MPU must to expect, when BF pass in 0 state.

Simultaneously with the BF reading on DB7 MPU become the address counter (AC) state on DB6-DB0. The AC address format coincide with the setting instructions of DDRAM/CGRAM address.

It should to have in view, that the AC address value can change during the implementation of some instructions (i.e. at BF=1), accompanied by the address change (for example, data read/write, cursor moving, display clear instructions et al.).

The writing procedure of Busy Flag is destined only for determination of the controller current state and is not the instruction, as do not change the controller state and do not require of an execution (execution time is 0).

Data Write to CGRAM and DDRAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
		MSB							**LSB**

The instruction is write the 8-bit data in DDRAM or CGRAM to AC current address. The data destination selection for the writing in DDRAM or CGRAM is implemented by previous instruction of DDRAM or CGRAM address setting. After data writing the AC addresses are automatically incremented or decremented according to the ID bit state of the "Data input set mode" instruction. According with that occur the cursor shift on the display to the right or to the left. Also simultaneously with the data writing in DDRAM (but not in CGRAM!) it can occur the display shift in an opposite side, if it is enabled by S bit of "Data input mode set" previous instruction.

Data Read from CGRAM or DDRAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
		MSB							**LSB**

It is an instruction for the reading of 8-bit data from DDRAM or CGRAM on the AC current address. The selection between DDRAM and CGRAM is realized by previous instruction of the setting of DDRAM address or CGRAM address.

The data reading procedure from memory is occurs in two stages. After any instruction execution DDRAM/CGRAM data is put into output data register. This is guaranteed that in output data register always will be contained the data of the current address, even if it was changed during the last instruction execution. At a time of the reading instruction execution at the E signal high level, the data from the output register are transferred DB interface. And then at E fall edge occur the incrementing or decrementing of AC address according to the ID bit state of "Input data state mode", and also the data reading on the AC new address from memory into the output register.

At the data reading the display shift is not occurs.

The automatic incrementing or decrementing of AC address bring, particularly, to the situation, when just now written data it is not possible at once to read, as the memory reading will be occur already on the new address. For it implementation it is necessary before reading to give the address or the cursor shift set instruction for the return of the AC previous value.

3. Controller internal memory

3.1. Displayed Data RAM (DDRAM)

The Displayed Data RAM (DDRAM) store the characters codes, displaying in the LCD screen. The character code – the 8-bit character number in the coding table of the character generator.

In the write/read mode, the access to the DDRAM is made on the current AC address. The DDRAM addressing depends from the displaying characters format and from the character lines number on display. The character code, read from DDRAM combined with the current COM line number and the CGROM page flag is used in the process of the information refresh on the screen for the character generator (CGROM or CGRAM) address driving. The character coding information, delivered from the character generator, is displayed directly on LCD screen.

3.2. Character generator (CGROM)

In the character generator mask ROM on the works – manufacturer is implemented the mask option from the characters set, displayed by the controller on the display screen. There are possible two formats of the characters formats: 5x8, 5x11. The first two character formats are named "standard" and can displayed on the screen simultaneously.

The SA3070B controller contents two CGROM. An each bank can program by the characters of any format. In the general case three coding variants are possible:

The characters 8-bit code, used by controller, allow to displays simultaneously on the screen in all up to 256 characters, which placed in the code tables. An each character of the code table locate on the crossing of the column and line, which numbers together put the 8-bit character code. From all tables for CGROM can be assigned:

- For the standard coding - 240 characters codes, accordingly some more 16 or 8 characters codes are destined for the character generator RAM (CGRAM).

At the standard characters coding:

An each CGROM assembly consists from 248 cells of the characters of 5x16 format. In the each cell two characters of 5x8 format or one character of 5x11 format can be write. There are some distinctions in the address driving method for the 5x8 and 5x11 characters at theirs access from CGROM (see Tables 12 and 13). In the coding table the columns range is stand out for the allocation of two pages of 5x8 characters from Amin up to Amax.

One should to note, that in one-line mode with the 1/8 sweep 1/8 (N=0 and F=0), and also in two-line mode the 5x11 are displayed in the truncated form – only overhead COM 8 lines. On other hand, under the 1/11 sweep mode (i.e. on COM 11 active lines) the characters of 5x8 format with two-page coding are augmented by the spaces in 9, 10 and 11 COM lines, providing the correct displaying (see Table 13).

Table 12. CGROM addressing and the characters 5x8 coding

CGROM Address												Data					
Character code								PG	COM[1..8]								
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_4	Q_3	Q_2	Q_1	Q_0	
0	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	
								0	0	0	1	1	0	0	0	0	
								0	0	1	0	1	0	1	1	0	
								0	0	1	1	1	1	0	0	1	**First page**
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	1	1	1	1	0	
								0	1	1	1	0	0	0	0	0	←Cursor position
								1	0	0	0	1	0	0	0	0	
								1	0	0	1	1	0	0	0	0	
								1	0	1	0	1	1	1	1	0	
								1	0	1	1	1	0	0	0	1	**Second page**
								1	1	0	0	1	0	0	0	1	
								1	1	0	1	1	0	0	0	1	
								1	1	1	0	1	1	1	1	0	
								1	1	1	1	0	0	0	0	0	←Cursor position

Notes:
1. Character code, corresponding to the addresses A_{11}-A_4, is selected from DDRAM (D7-D0) according to the character position on the display.
2. A_2-A_0 addresses– COM[1..8] character line number.
3. Pixel background on the screen corresponds to 1 state in CGROM.

Table 13. CGROM addressing and the characters 5x11 coding

CGROM address												Data					
Character code								COM [1..11]									
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_4	Q_3	Q_2	Q_1	Q_0	
0	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	
								0	0	0	1	1	0	0	0	0	
								0	0	1	0	1	0	1	1	0	
								0	0	1	1	1	1	0	0	1	**First page**
								0	1	0	0	1	0	0	0	1	**or**
								0	1	0	1	1	0	0	0	1	**Second page**
								0	1	1	0	1	1	1	1	0	
								0	1	1	1	0	0	0	0	0	At 1/11 sweep the 5x8 character is supplemented with"0" in 9, 10 and 11 lines
								1	0	0	0	0	0	0	0	0	
								1	0	0	1	0	0	0	0	0	
								1	0	1	0	0	0	0	0	0	←Cursor position
								1	0	1	1	*	*	*	*	*	
								1	1	0	0	*	*	*	*	*	
								1	1	0	1	*	*	*	*	*	
								1	1	1	0	*	*	*	*	*	
								1	1	1	1	*	*	*	*	*	
1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	
								0	0	0	1	0	0	0	0	0	
								0	0	1	0	0	1	1	0	1	
								0	0	1	1	1		0	1	1	
								0	1	0	0	1	0	0	0	1	**First page**
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	0	1	1	1	1	
								0	1	1	1	0	0	0	0	1	
								1	0	0	0	0	0	0	0	1	
								1	0	0	1	0	0	0	0	1	
								1	0	1	0	0	0	0	0	0	←Cursor position
								1	0	1	1	*	*	*	*	*	
								1	1	0	0	*	*	*	*	*	
								1	1	0	1	*	*	*	*	*	
								1	1	1	0	*	*	*	*	*	
								1	1	1	1	*	*	*	*	*	

Notes:

1. Character code, corresponding to the addresses A_{11}-A_4, is selected from DDRAM (D7-D0) according to the character position on the display.
2. A_3-A_0 addresses– COM[1..11] character line number.
3. 5x8 characters are supplemented from below with "0" COM [9..11] lines.
4. Characters from one-page outside the (Amin-Amax) addresses range are coded completely in 11 lines.
5. Data in COM[12..16] lines are not displayed on the screen and not have significance.
6. 4 Pixel background on the screen correspond to 1 state in CGROM.

3.3. Character generator RAM (CGRAM)

In the character generator RAM (CGRAM) the user can write on the program base own characters: 8 characters of 5x8 format or 4 characters of 5x11 format. The correspondence of the CGRAM addresses and character coding is shown in Table 9 for characters 5x8 and in Table 10 for characters 5x11.

The CGRAM cell, containing information about one 5x8 character code occupies 8 bytes. The characters are written by the line, an each byte contain the information about one character line, at that only 5 low order bits D4-D0 are used for displaying. 3 high order bits D7-D5 are not displaying on the screen and can be used for the storing of general-purpose data. The CGRAM capacity is 64 bytes and in it possible to write successively 8 characters of 5x8 format.

When writing the characters of 5x11 format an each character occupies incomplete two 8-byte CGRAM cells. In the second cell 9, 10 & 11-character line are coded. The information from next 5 byte from CGRAM is not displayed on the screen, therefore can contain the random general-purpose data. The CGRAM characters of 5x11format codes, written in DDRAM, will be numbered every other one in 00h-07h code range, for example, if the first character is written from CGRAM 0 cell, occupying 0 and 1 cells, it is possible to use 00h, 02h, 04h & 06h codes to display such 4 characters.

Note: When using 5x11 font mode, 5x8 characters must be coded completely in 11 lines with spaces in 9, 10, and 11 lines, because the function of the automatic spaces filling, used in two-page CGROM coding, does not work with CGRAM.

In the controller standard mask option variant for 8 characters of CGRAM are used 16 codes, at that the CGRAM characters are repeated twice – for 00h-07h and 08h-0Ah codes. In more advanced variant in CGRAM is used only 00h-07h codes range. Accordingly for CGROM 8 character codes (08h-0Fh) are extracted extra, increasing theirs general quantity up to 248.

In Tables 15, 16 and 17 the complete A11-A0 address is indicated, which used at the addressing of character generator (both CGROM, as well as CGRAM), and the AC address, corresponding to it, used for the access through the MPU interface.

Table 15. CGRAM addressing for 5x8 characters

CGRAM selection sign								CGRAM Address				Data								
Character code								COM[1..8]												
AC_5 AC_4 AC_3								AC_2 AC_1 AC_0												
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	
0	0	0	0	*	0	0	0	*	0	0	0	*	*	*	1	1	1	1	0	
								*	0	0	1	*	*	*	1	0	0	0	1	
								*	0	1	0	*	*	*	1	0	0	0	1	
								*	0	1	1	*	*	*	1	1	1	1	0	First
								*	1	0	0	*	*	*	1	0	1	0	0	Character
								*	0	0	1	*	*	*	1	0	0	1	0	
								*	1	0	0	*	*	*	1	0	0	0	1	
								*	1	0	1	*	*	*	0	0	0	0	0	←Cursor position
0	0	0	0	*	0	0	1	*	0	0	0	*	*	*	1	0	0	0	1	
								*	0	0	1	*	*	*	0	1	0	1	0	
								*	1	0	0	*	*	*	1	1	1	1	1	
								*	1	0	1	*	*	*	0	0	1	0	0	Second
								*	0	0	0	*	*	*	1	1	1	1	1	character
								*	0	0	1	*	*	*	0	0	1	0	0	
								*	0	1	0	*	*	*	0	0	1	0	0	
								*	0	1	1	*	*	*	0	0	0	0	0	←Cursor position

Notes:
1. Character code, corresponding to the address A_{11}-A_4, is chosen from DDRAM (D7-D0) according to the character position on the display.
2. Addresses A_{11}-A_7 of the character generator are the sign of CGRAM access (A_{11}-A_7=0000*). Address A_7 is not usually used, that means, CGRAM access for 00h-0Fh codes. However, it may be additionally determined, at that A_7=0 will mean access of CGRAM (8 codes 00h-07h), A_7=1 – access of CGROM (additional 8 codes 08h-0Fh).
3. Addresses A_6-A_4 – CGRAM character code (3 addresses, in all 8 characters 5x8).
4. Address A_3 – not used to display 5x8 characters.
5. Addresses A_2-A_0 – COM[1..8] character line number.
6. AC_5-AC_0 – the address counter (AC) bits while read/write data operation.
7. Pixel background on the screen correspond to the state 1 in CGRAM.
8. CGRAM Q_7-Q_5 bits are not displaying on the screen can be used for the storing of the general-purpose data.

Table 16. CGRAM addressing for 5x11 characters

CGRAM access flag								CGRAM Address																
Character code								COM[1..11]																
AC_5 AC_4								AC_3	AC_2		AC_1	AC_0												
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3		A_2		A_1		A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	
0	0	0	0	*	0	0	*	0	0		0	0			*	*	*	0	0	0	0	0	
								0	0		0	1			*	*	*	0	0	0	0	0	
								0	0		1	0			*	*	*	1	0	1	1	0	
								0	0		1	1			*	*	*	1	1	0	0	1	First
								0	1		0	0			*	*	*	1	0	0	0	1	character
								0	0		0	1			*	*	*	1	0	0	0	1	
								0	1		0	0			*	*	*	1	1	1	1	0	
								0	1		0	1			*	*	*	1	0	0	0	0	
								1	0		0	0			*	*	*	1	0	0	0	0	
								1	0		0	1			*	*	*	1	0	0	0	0	
								1	1		0	0			*	*	*	0	0	0	0	0	←cursor position
								1	1		0	1			*	*	*	*	*	*	*	*	
								1	0		0	0			*	*	*	*	*	*	*	*	
								1	0		0	1			*	*	*	*	*	*	*	*	
								1	0		1	0			*	*	*	*	*	*	*	*	
								1	0		1	1			*	*	*	*	*	*	*	*	
0	0	0	0	*	0	1	*	0	0		0	0			*	*	*	0	0	0	1	0	
								0	0		0	1			*	*	*	0	0	0	0	0	
								0	0		1	0			*	*	*	0	0	1	1	0	
								0	0		1	1			*	*	*	0	0	0	1	0	Second
								0	1		0	0			*	*	*	0	0	0	1	0	character
								0	0		0	1			*	*	*	0	0	0	1	0	
								0	1		0	0			*	*	*	0	0	0	1	0	
								0	1		0	1			*	*	*	0	0	0	1	0	
								1	0		0	0			*	*	*	1	0	0	1	0	
								1	0		0	1			*	*	*	0	1	1	0	0	
								1	1		0	0			*	*	*	0	0	0	0	0	←cursor position
								1	1		0	1			*	*	*	*	*	*	*	*	
								1	0		0	0			*	*	*	*	*	*	*	*	
								1	0		0	1			*	*	*	*	*	*	*	*	
								1	0		1	0			*	*	*	*	*	*	*	*	
								1	0		1	1			*	*	*	*	*	*	*	*	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…

Notes:
1. Character code, corresponding to the A_{11}-A_4 addresses, is accessed from DDRAM (D7-D0) according to the character position on the display
2. Addresses A_{11}-A_7 of the character generator are the access sign of (A_{11}-A_7=0000*). The address A_7 is not usually used, that means the CGRAM access for 00h-0Fh codes. However, it may be additionally determined, at that A_7=0 will mean CGRAM access (8 codes in the 00h-07h range), A_7=1 – CGROM access (additional 8 codes (08h-0Fh).
3. Addresses A_6-A_4 – CGRAM character code (3 addresses, in all 4 characters 5x11).
4. Address A_4 – not used for the displaying characters 5x11.
5. Addresses A_2-A_0 – character line COM[1..11] number.
6. AC_5-AC_0 – address counter (AC) bits while the read/write operations.
7. Pixel background on the screen corresponds to the state 1 in CGRAM.
8. CGRAM Q_7-Q_5 bits and 12-16 bytes of each character are not displaying on the screen and can be used for the storing of the general-purpose data.

4. Drivers subsystem for the LCD screen control

4.1. Panel LCD interface

The LCD screen is a matrix consisting of lines and columns on which crossings there are active elements. The matrix lines are connected to COM[1:16] controller outputs, and columns – to SEG controller outputs and extension drivers.

The multiplexing method is used for the information display, i.e. dynamic sharing of the displaying information in time. In every moment of time the information set on the controller SEG outputs is highlighted only for one active COM - line. After a time period equal to the line refresh period, the next COM become active, for which on the SEG outputs is set the appropriate information. For time, equal to the screen refresh, it is an activation of all COM lines, forming the characters. It is supposed, that the screen element state, installed during it activation, is hold at least on the period of the refresh of all screen.

The controller can form three variants of timing diagram with the multiplexing level 1/8, 1/11, 1/16 (see Table 20). The number in denominator shows the amount of active COM lines, remaining COM lines are always passive, and the screen elements, connected to theirs – not highlighted.

The activity of COM lines is determined by the counter-decoder, which in series search all COM lines up to maximum value, determined by the appropriate display sweep mode.

Table 20 Screen sweeps formats

Lines number	Character size	Number of active COM lines	Multiplexing level
1	5x8	8	1/8
1	5x11	11	1/11
2	5x8	16	1/16

4.2. Characters generator output data writing to drivers SEG shift registers

The information about displayed characters is transferred into the shift register in reverse order, i.e. for each COM line at first the data for last character are transferred, then the address is decreased and the information is transferred for previous character etc. (for example, see Figures 4 and 5 for one-line mode and Figures 6 and 7 for two-line mode). The number of the last line character, which is first loaded into the shift register is set by the start refresh address counter (see part 2.5. "Start Refresh Address Counter and Display Shifting") The first 16 characters of line are always displayed by mans of the controller SEG drivers (totally 80 SEG outputs), for theirs the data are received at the end of COM – line update cycle.

After filling the shift register with the data for next COM line is given CLK1 pulse, on the falling edge of which the data from shift register are written into output SEG latches and displayed on the screen simultaneously with switching to new COM, and shift register start to filled by the data for next COM line. Thus, CLK1 pulse is a line frequency synchronization signal of the display sweep.

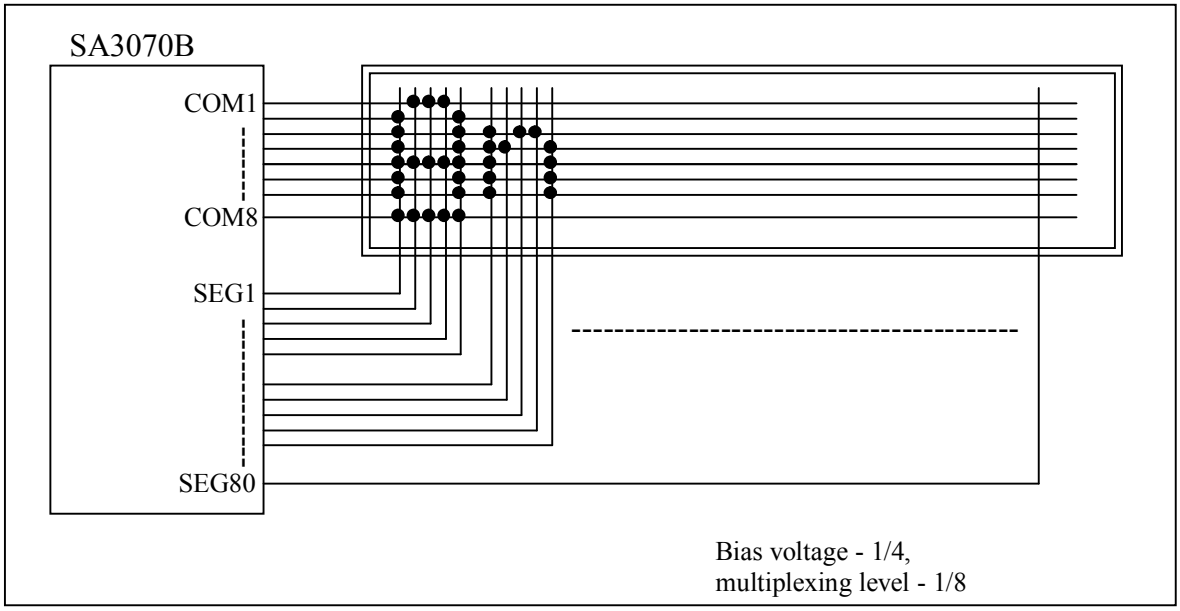


Figure 12.Example of 16 characters 5x8 in one line.

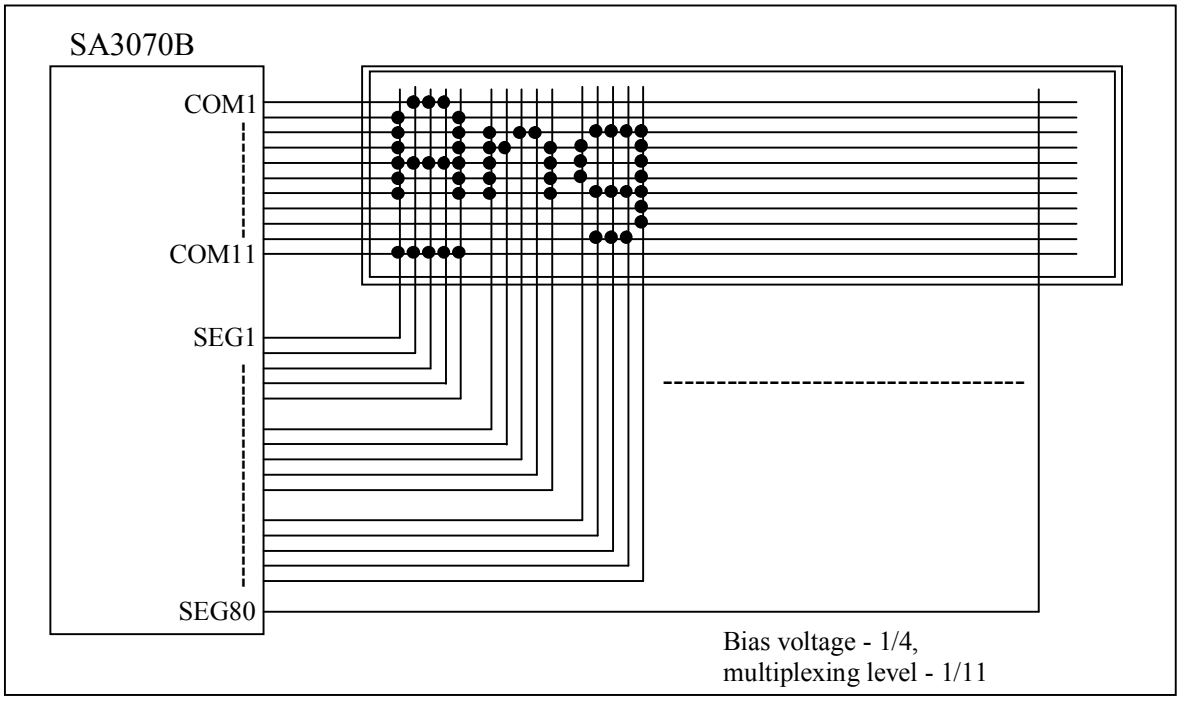


Figure 13. Example of one line 16 characters 5x11

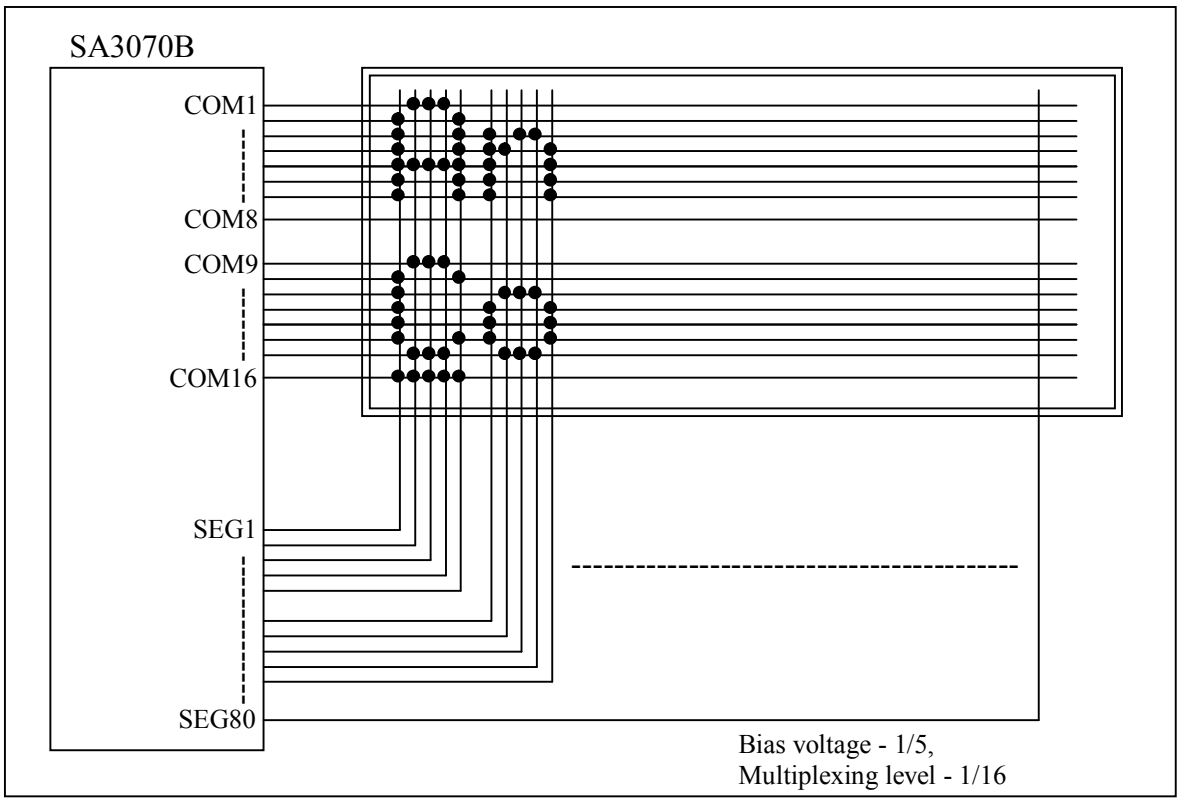


Figure 14. Example of two lines in 16 characters 5x8

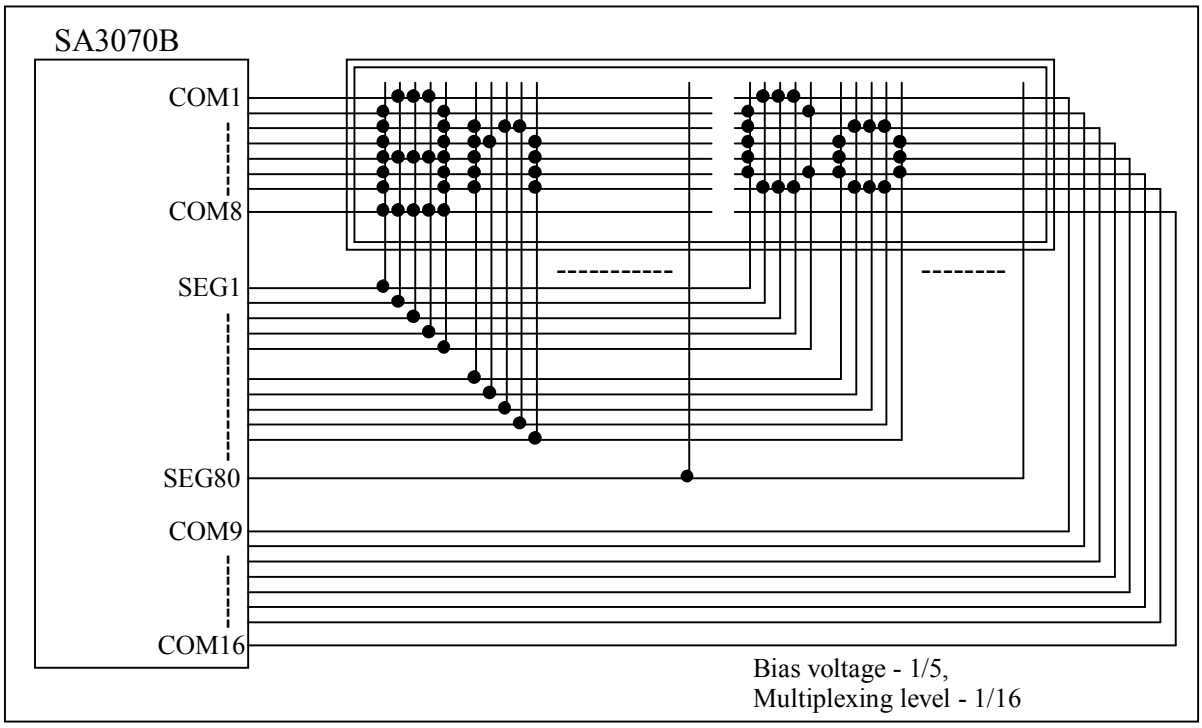


Figure 15. Example of one line 16 characters 5x8 in one line.

5. Controller programming

5.1. Controller program initialization

Program initialization in 8-bit interface mode

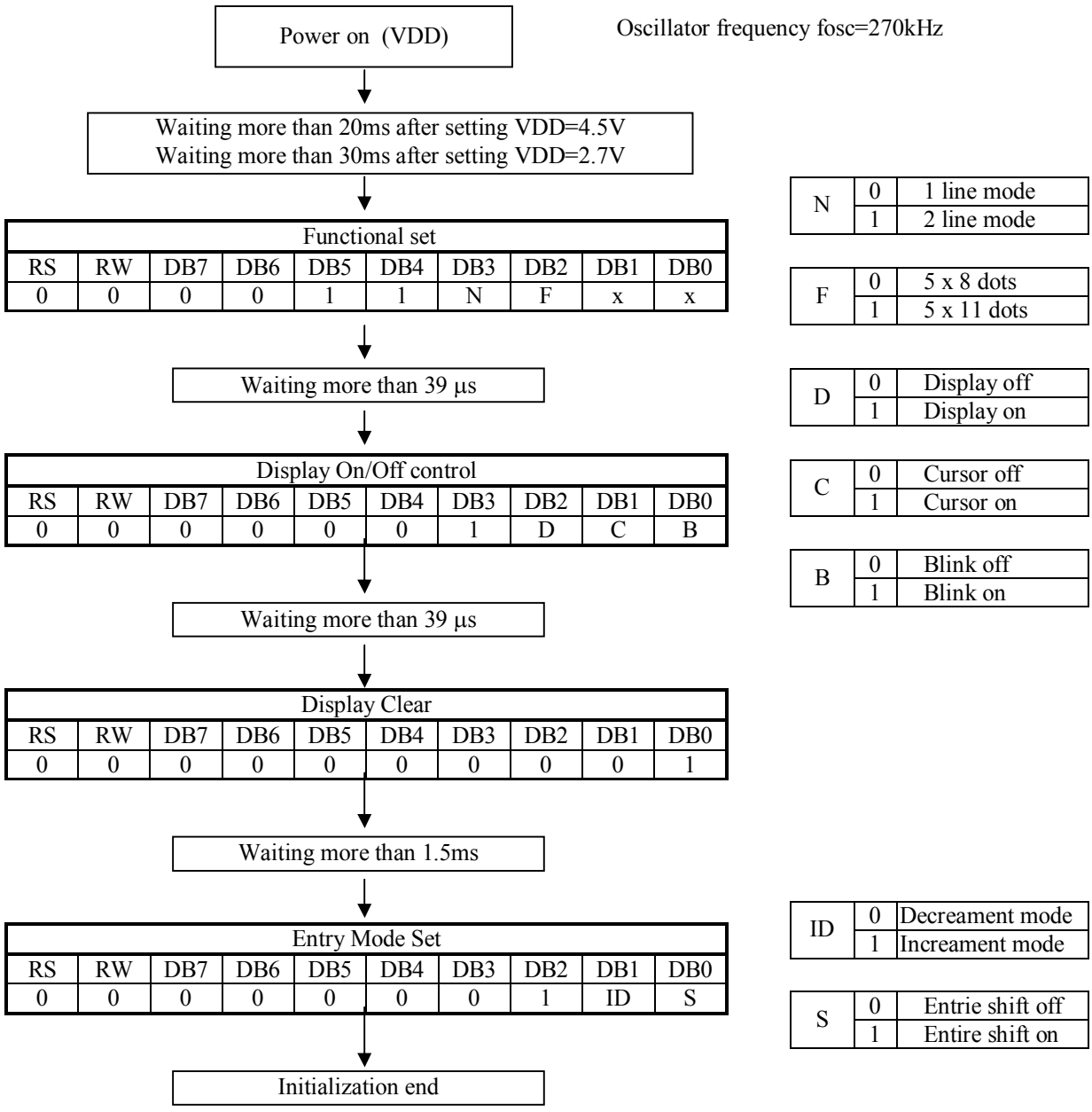


Figure 25. Controller program initialization in 8-bit interface mode

Program initialization in 4-bit interface mode

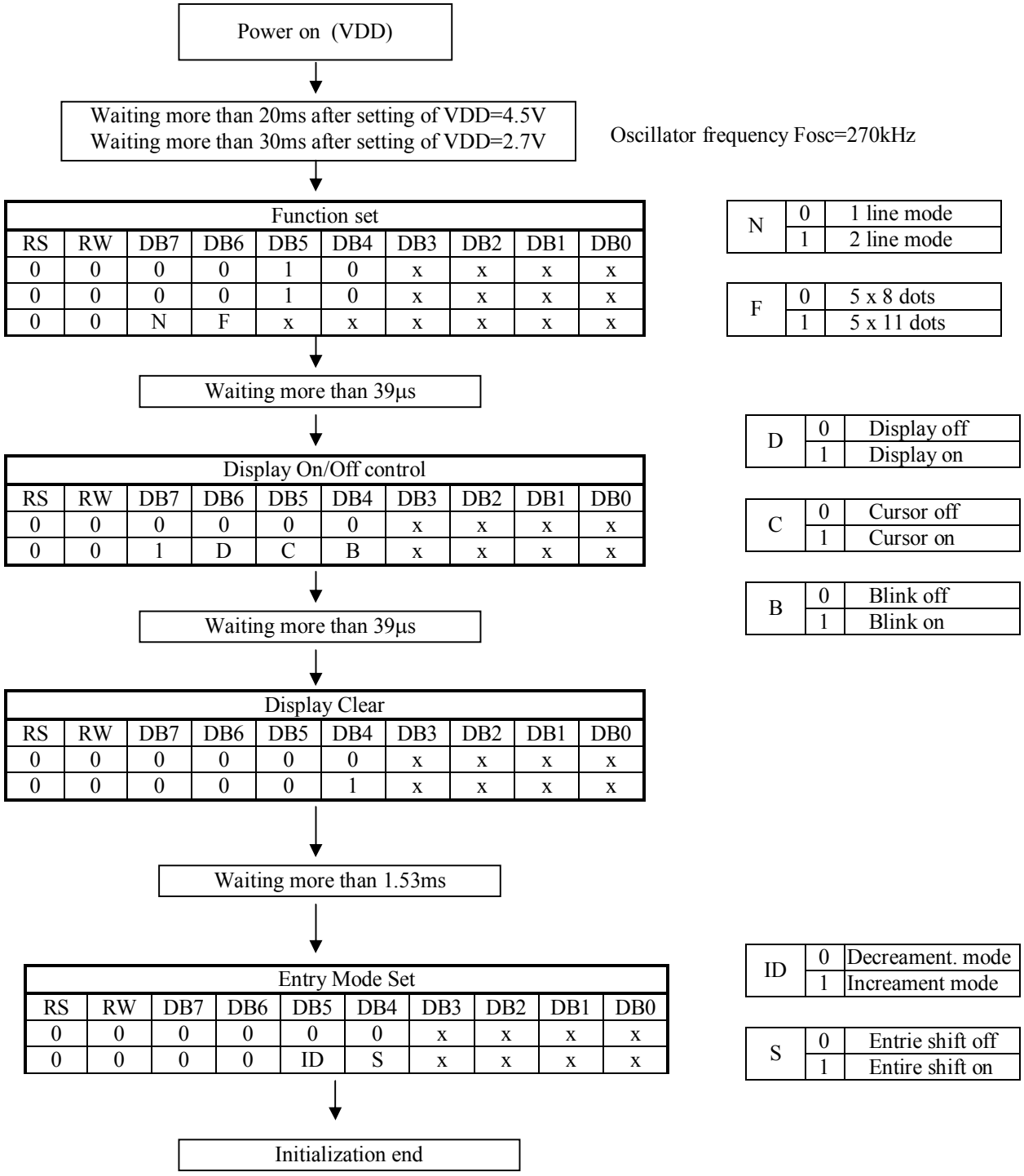


Figure 26. Controller initialisation in 4-bit interface mode

5.2. Example of controller programming in 8-bit interface mode

Instructions sequence **LCD panel**

1. Power On: internal initialisation from the start reset circuit

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

2. Functional state set: 8 bit, 2 lines, 5x8 font

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	*	*

3. Display On, cursor on, blinking off

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	1	0

LCD panel: _

4. Input data mode set: address incrementing

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	0

LCD panel: _

5. Data writing: character D

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	0	0

LCD panel: D_

6. Data writing: character R

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	0

LCD panel: DR_

7. Data writing: character A

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	0	1

LCD panel: DRA_

8. Data writing: character G

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	1	1

LCD panel: DRAG_

9. Data writing: character O

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	1

LCD panel: DRAGO_

10. Data writing: character N

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	0

LCD panel: DRAGON_

11. DDRAM address set: 40h

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	0	0	0

LCD panel:
DRAGON
_

12. Data writing: character S

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

LCD panel:
DRAGON
S_

13. Data writing: character A

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	0	1

LCD panel:
DRAGON
SA_

14. Data writing: character 3

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	1	1

LCD panel:
DRAGON
SA3_

15. Data writing: character 0

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

```
DRAGON
SA30_
```

16. Data writing: character 7

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	1	1

```
DRAGON
SA307_
```

17. Data writing: character 2

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	1	0

```
DRAGON
SA3072_
```

18. Cursor or Display Shift: Cursor shift left

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	0	*	*

```
DRAGON
SA3072
```

19. Data writing: character 0

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

```
DRAGON
SA3070B_
```

20. Data writing: character B

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	1	0

```
DRAGON
SA3070B_
```

21. Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	*

```
DRAGON
SA3070B
```

22. Clear Display

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

```
_
```

5.3. Example of controller programming in 4-bit interface

Instructions sequence **LCD panel**

1. Power On: internal initialization from start reset circuit

RS	RW	DB7	DB6	DB5	DB4

2. Functional state set: 4 bit, 2 lines, 5x8 font

RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	1	0
0	0	0	0	0	0

3. Display On, Cursor On, Blinking Off

RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	0	0
0	0	1	1	1	0

4. Data Input Mode: Address incrementing

RS	RW	DB7	DB6	DB5	DB4
0	0	0	0	0	0
0	0	0	1	1	0

5. Data writing: character D

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	0	1	0	0

6. Data writing: character R

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	1
1	0	0	0	1	0

7. Data writing: character A

RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	0	0	0	1

8. Data writing: character G

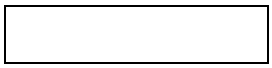
RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	0	1	1	1

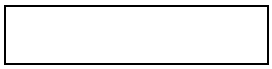
9. Data writing: character O

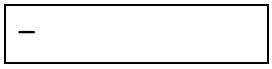
RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	1	1	1	1

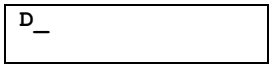
10. Data writing: character N

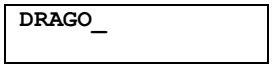
RS	RW	DB7	DB6	DB5	DB4
1	0	0	1	0	0
1	0	1	1	1	0

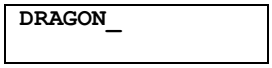






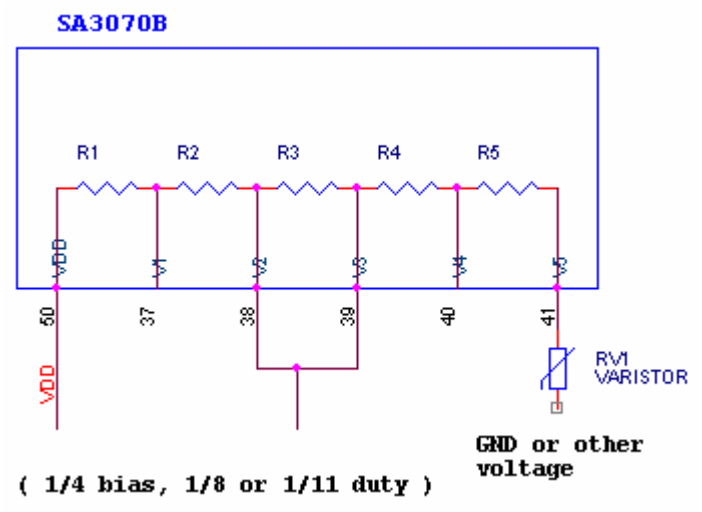


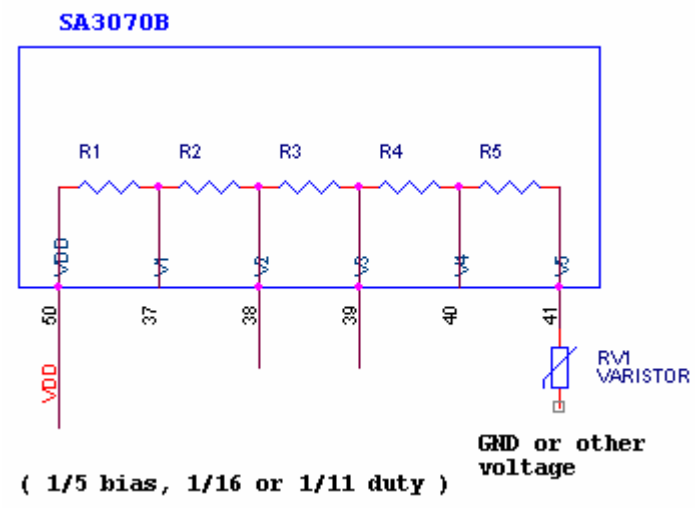




6. Bias Voltage Divide Circuit

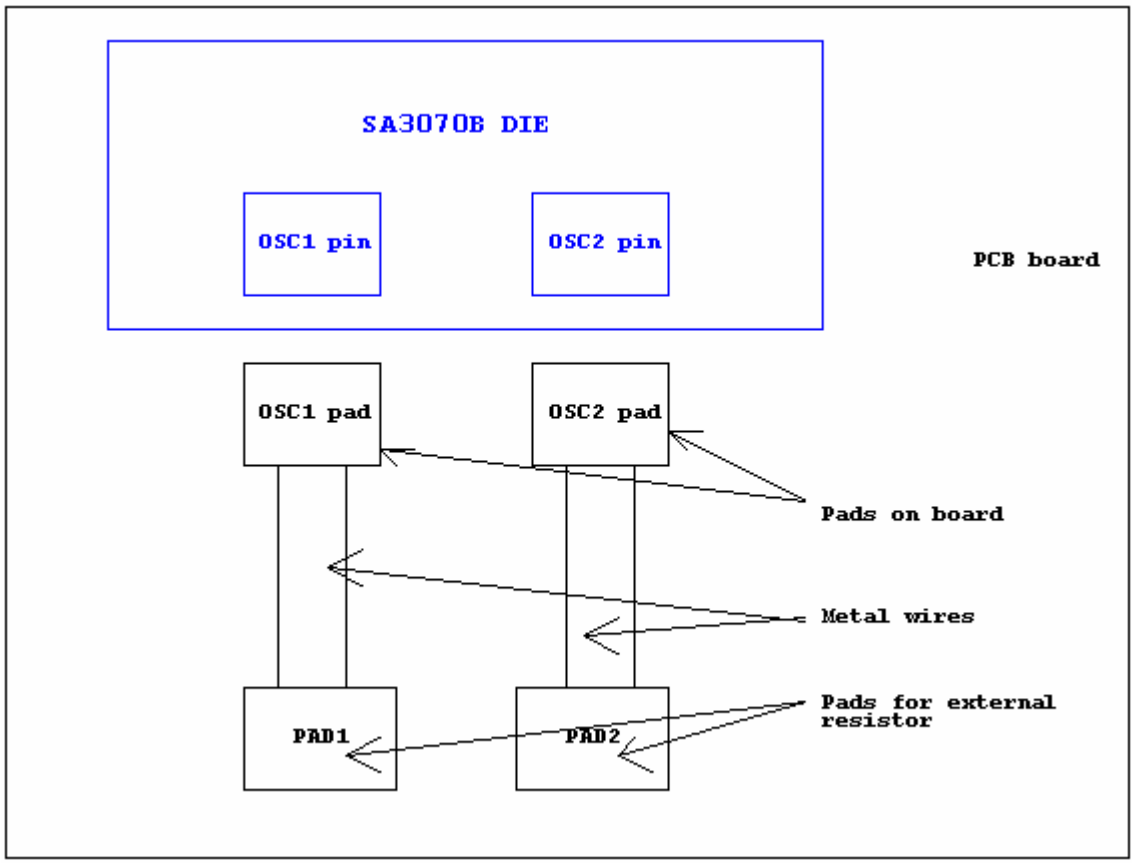
Built-in resistors type



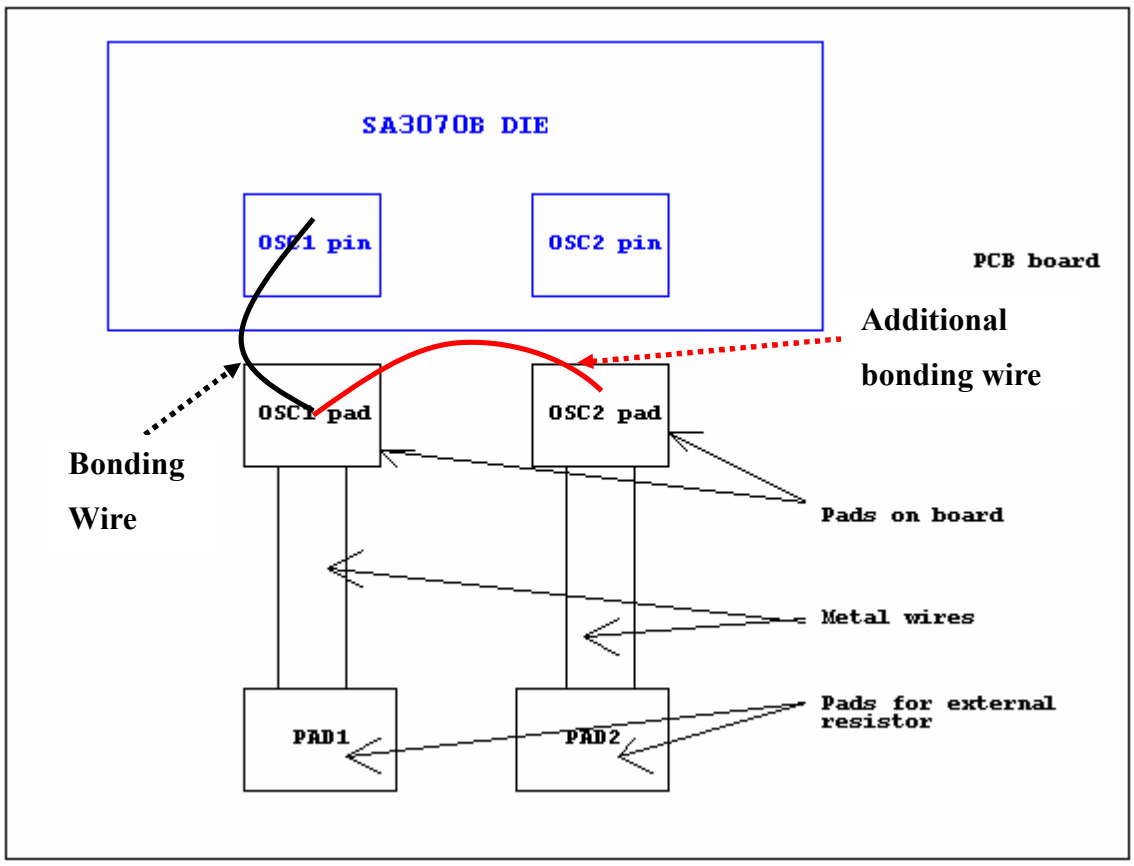


7. OSC Frequency Adjusting (*For Built-in resistors type)

The first application VDD=3V (not bonding at all)



The second application VDD=5V (with bonding)



Bonding wire, metal wire, OSC1 and Pad1 pads on board have some capacitance. And this additional capacitance will decrease oscillator frequency at this application mode. To increase the capacitance it is possible to use additional bonding wire (one of the red wires).

8. Initializing

When the power is turned on, SA3070B is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High" (busy state) to the end of initialization.

i. "Display Clear" instruction writes "0x20" to all DDRAM

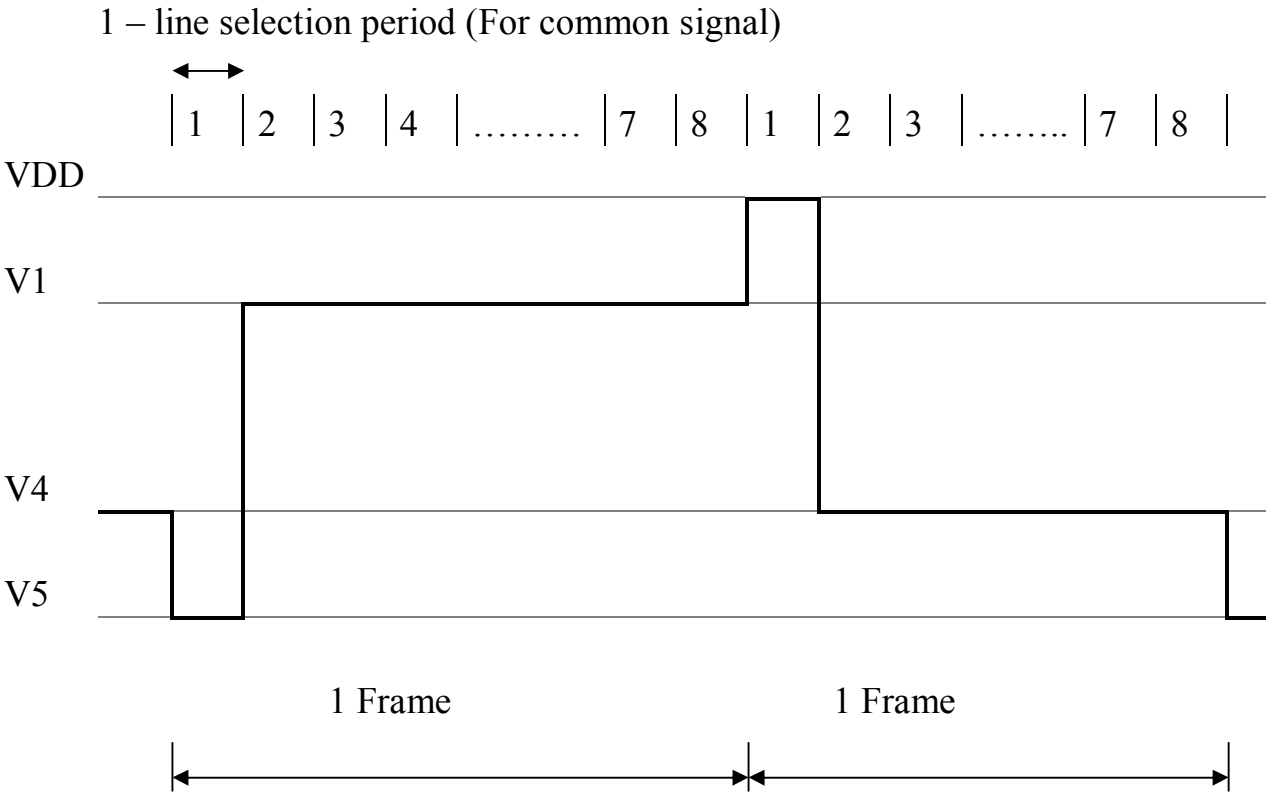
ii. "Function Set" instruction
DL=1: 8-bit bus mode
N=0: 1-line display mode
F=0: 5x8 font type

iii. "Display ON/OFF" instructions
D=0: Display OFF
C=0: Cursor OFF
B=0: Blink OFF

iv. "Entry Mode Set" instruction
I/D=1: Increment by 1
SH=0: No entire display shift

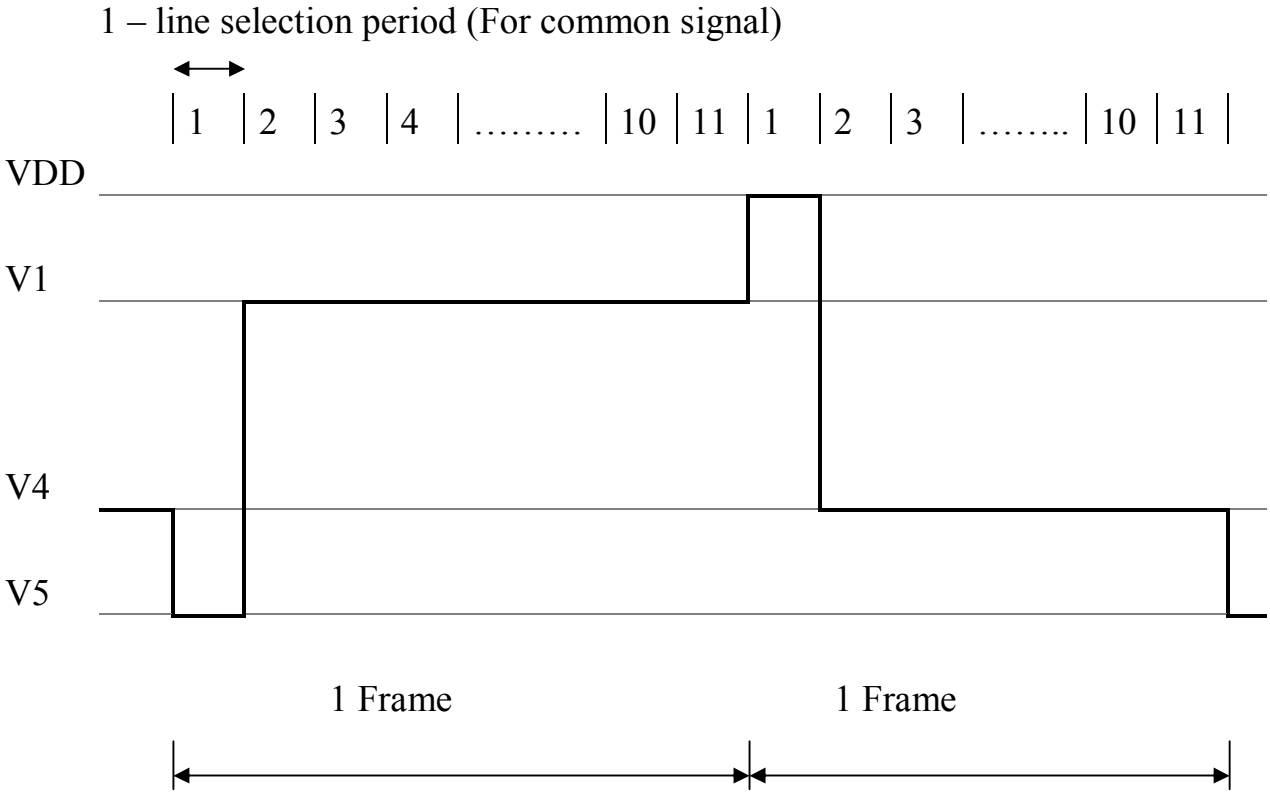
9. Frame Frequency

1.) 1/8 duty cycle



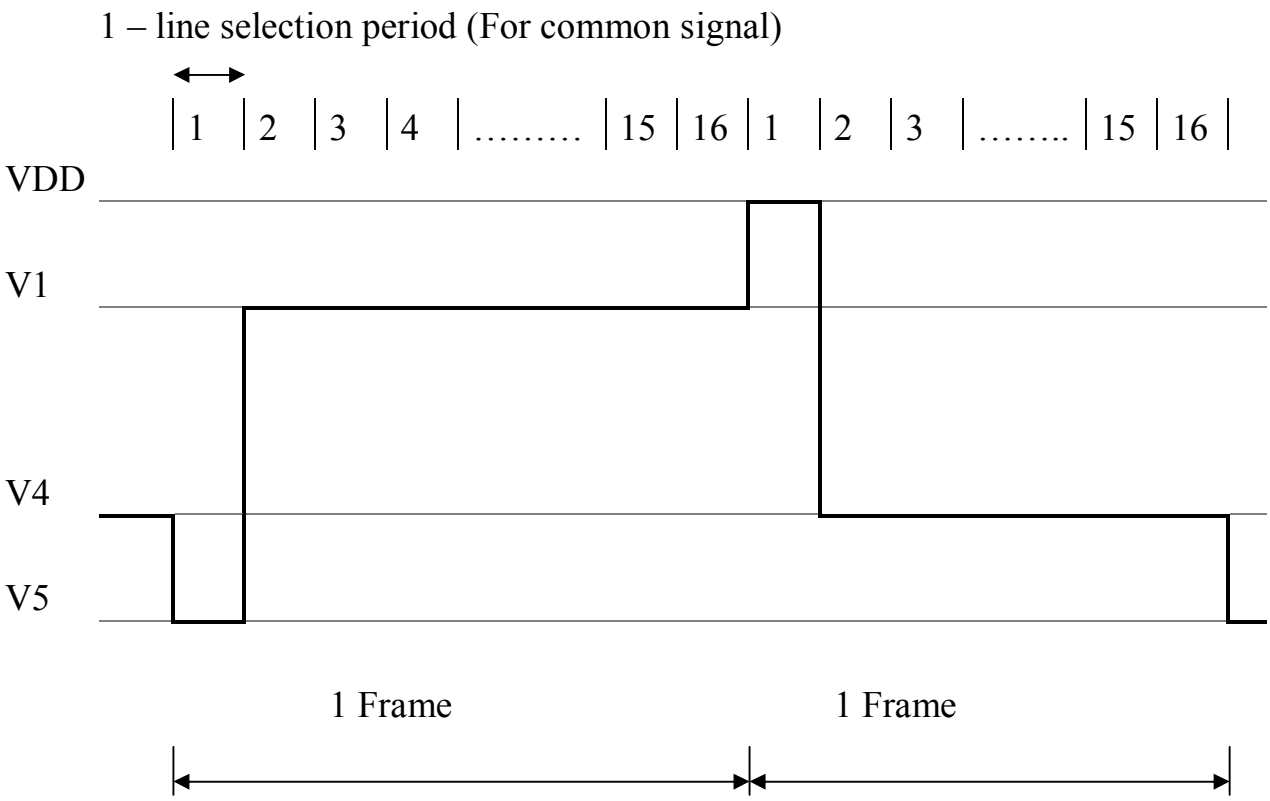
Line selection period = 400 clocks
One Frame 400 x 8 x 3.7us = 11850us = 11.9ms (1 clock=3.7us, fosc=270kHz)
Frame frequency = 1/11.9ms = 84.03Hz

2.) 1/11 duty cycle



Line selection period = 400 clocks
One Frame 400 x 11 x 3.7us = 16300us = 16.3ms (1 clock=3.7us, fosc=270kHz)
Frame frequency = 1/16.3ms = 61.4Hz

3.) 1/16 duty cycle



Line selection period = 200 clocks
One Frame 200 x 16 x 3.7us = 11850us = 11.9ms (1 clock=3.7us, fosc=270kHz)
Frame frequency = 1/11.9ms = 84.03Hz

10. Controller electrical characteristics

10.1. Absolute Maximum Ratings

Parameter	Symbol	Unit	Value
Power supply voltage	V_{DD}	V	From -0.3 up to 7.0
Power supply voltage	V_{LCD}	V	From VDD-15.0 up to VDD+0.3
Input voltage	V_{IN}	V	From -0.3 up to VDD+0.3

Note: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$.

10.2. Temperature ratings

Parameter	Symbol	Unit	Value
Operating temperature range	Topr	℃	From -30 up to +85
Storage temperature range	Tstg	℃	From -55 up to +125

10.3. Electrical characteristics for V_{DD} = 4.5V - 5.5V

(V_{DD}=4.5V - 5.5V, Ta= +25 ℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operation voltage	VDD	-	4.5		5.5	V
Operation current	IDD	Internal oscillation or external clock (VDD = 5.0V, fosc = 270k Hz)	-	0.3	0.6	mA
Input voltage (1) (expect OSC1)	V_{IH1}	-	2.2	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.6	
Input voltage (2) (OSC1)	V_{IH2}	-	VDD-1.0	-	VDD	
	V_{IL2}	-	-0.2	-	1.0	
Output voltage (1) (DB7-DB0)	V_{OH1}	I_{OH} = 0.25mA	2.4	-	-	V
	V_{OL1}	I_{OL} = 1.2mA	-	-	0.4	
Output voltage (2) (expect DB7-DB0)	V_{OH2}	Io = -40μA	0.9VDD	-	0.4	
	V_{OL2}	Io = 40μA	-	-	0.1VDD	
Voltage drop	Vd_{COM}	I_O= ±0.1mA	-	-	0.2	V
	Vd_{SEG}				0.2	
Input leakage current	I_{LKG}	V_{IN}= 0V - V_{DD}	-1	-	1	μA
Input low current	IIL	VIN=0V, VDD =5V (Pull up)	-40	-100	-180	
Internal clock (no built-in resistors type)	fosc	Rf = 91kΩ±2% (VDD = 5V)	190	270	350	kHz
Internal clock (built-in resistors type)	fosc	Built-in resistor & bonding wire(VDD=5V)	190	270	350	kHz
LCD driving voltage	VLCD	VDD-V5 (1/5, 1/4 bias)	3.0	-	10.0	V

10.4. Electrical characteristics for V_{DD} = 2.7V - 4.5V

(V_{DD}=2.7V - 4.5V, Ta= +25 ºC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operation voltage	VDD	-	2.7		4.5	V
Operation current	IDD	Internal oscillation or external clock (VDD = 3.0V, fosc = 270k Hz)	-	0.15	0.3	mA
Input voltage (1) (expect OSC1)	V_{IH1}	-	0.7VDD	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.4	
Input voltage (2) (OSC1)	V_{IH2}	-	0.7VDD	-	VDD	
	V_{IL2}	-	-	-	0.2VDD	
Output voltage (1) (DB7-DB0)	V_{OH1}	I_{OH} = 0.1mA	0.75VDD	-	-	V
	V_{OL1}	I_{OL} = 0.1mA	-	-	0.2VDD	
Output voltage (2) (expect DB7-DB0)	V_{OH2}	Io = -40µA	0.8VDD	-	-	
	V_{OL2}	Io = 40µA	-	-	0.2VDD	
Voltage drop	Vd_{COM}	I_O= ±0.1mA	-	-	0.2	V
	Vd_{SEG}				0.2	
Input leakage current	I_{LKG}	V_{IN}= 0V - V_{DD}	-1	-	1	µA
Input low current	IIL	VIN=0V, VDD =3V (Pull up)	-10	-40	-90	
Internal clock (no built-in resistors type)	fosc	Rf = 75kΩ±2% (VDD = 3V)	190	270	350	kHz
Internal clock (built-in resistors type)	fosc	Built-in resistor & bonding wire (VDD=3V)	190	270	350	kHz
LCD driving voltage	VLCD	VDD-V5 (1/5, 1/4 bias)	3.0	-	10.0	V

11. Controller time parameters

11.1. Time parameters in range V_{DD} = 4.5V - 5.5V

(V_{DD}=4.5V - 5.5V, Ta= -30 - +85ºC)

Mode	Parameter	Symbol	Min.	Max.	Unit
Write Mode (Figure 27)	E Cycle Time	t_C	500		ns
	E Rise/Fall Time	t_r, t_f		25	
	E Pulse Width	t_W	220		
	RS and RW Pre-Setup Time relative to E	t_{SU1}	40		
	RS and RW Hold Time relative to E	t_{H1}	10		
	DB [7..0] Input Data Pre-Setup Time relative to E	t_{SU2}	60		
	DB [7..0] Input Data Hold Time relative to E	t_{H2}	10		
Read Mode (Figure 28)	E Cycle Time	t_C	500		ns
	E Rise/Fall Time	t_r, t_f		25	
	E Pulse Width	t_W	220		
	RS and RW Pre-Setup Time relative to E	t_{SU}	40		
	RS and RW Hold Time relative to E	t_H	10		
	DB[7..0] Output Data Delay Time relative to E	t_D		120	
	DB[7..0] Output Data Hold Time relative to E	t_{DH}	20		

11.2. Time parameters in range V_{DD} = 2.5V - 4.5V

(V_{DD}=2.5V - 4.5V, Ta= -30 - +85ºC)

Mode	Parameter	Symbol	Min.	Max.	Unit
Write Mode (Figure 27)	E Cycle Time	t_C	1000		ns
	E Rise/Fall Time	t_r, t_f		25	
	E Pulse Width	t_W	400		
	RS and RW Pre-Setup Time relative to E	t_{SU1}	60		
	RS and RW Hold Time relative to E	t_{H1}	20		
	DB[7..0] Input Data Pre-Setup Time relative to E	t_{SU2}	140		
	DB[7..0] Input Data Hold Time relative to E	t_{H2}	10		
Read Mode (Figure 28)	E Cycle Time	t_C	1000		ns
	E Rise/Fall Time	t_r, t_f		25	
	E Pulse Width	t_W	400		
	RS and RW Pre-Setup Time relative E	t_{SU}	60		
	RS and RW Hold Time relative E	t_H	20		
	DB[7..0] Output Data Delay Time relative to E	t_D		360	
	DB[7..0] Output Data Hold Time relative to E	t_{DH}	5		

11.3. Interface Timing Diagrams

Write operation

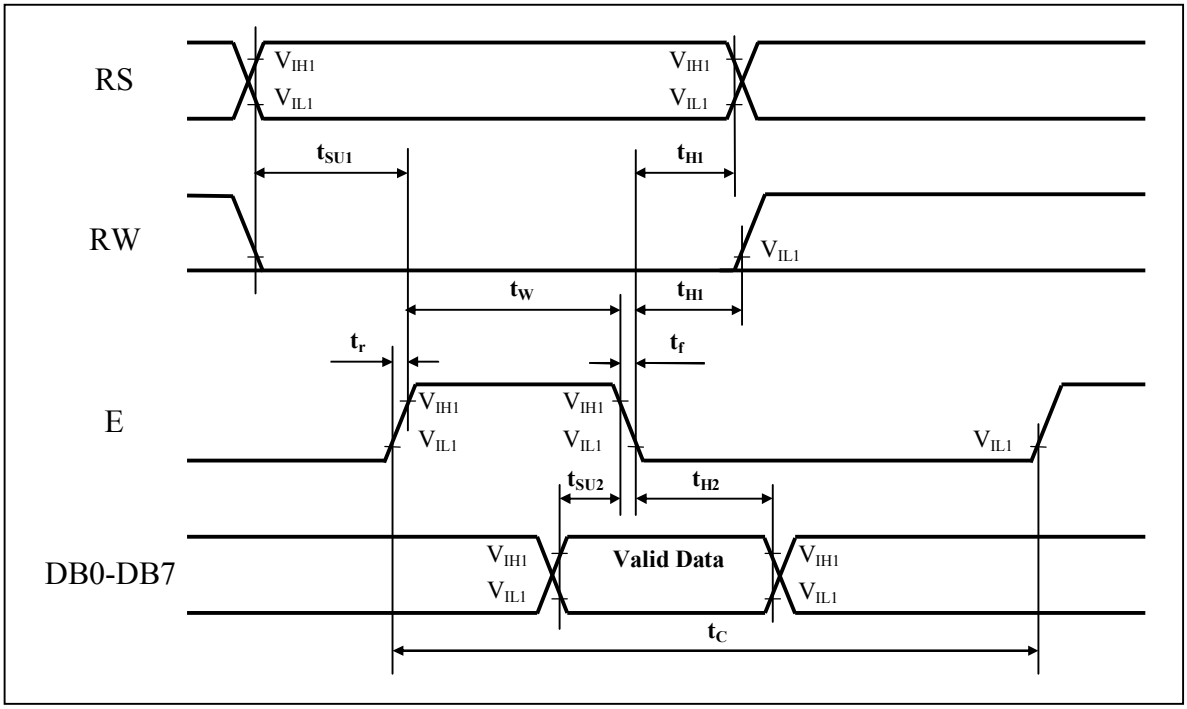


Figure 27. Write Mode Timing Diagram

Read operation

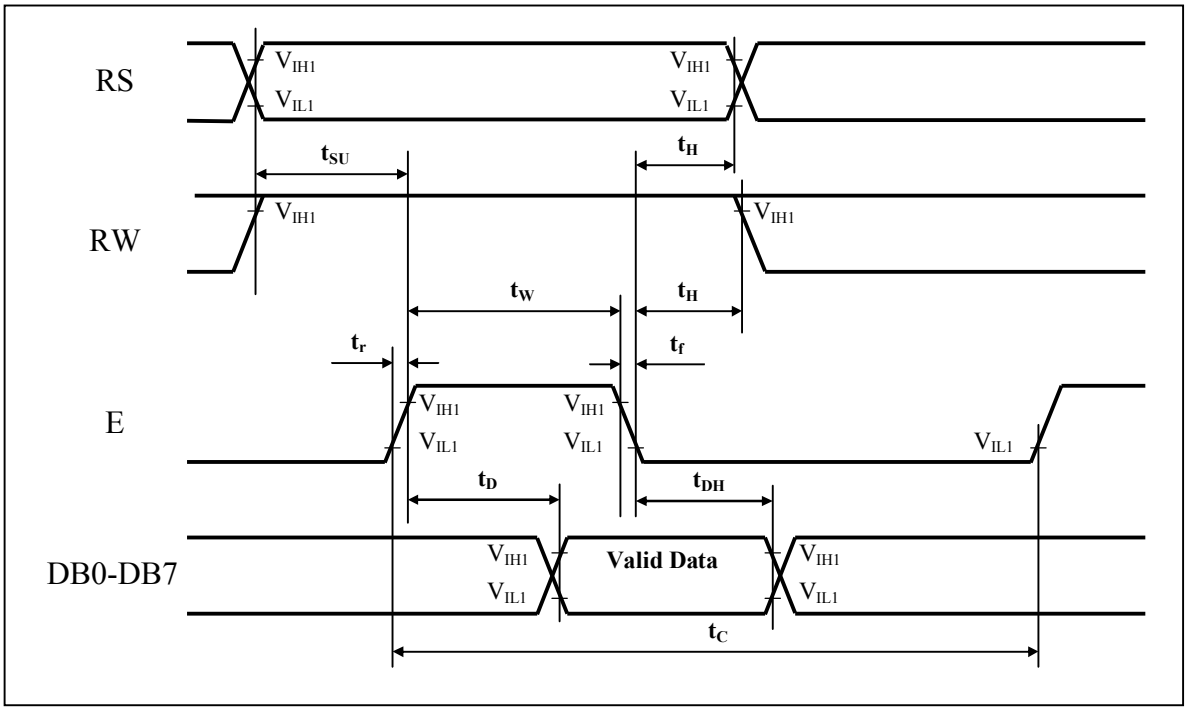
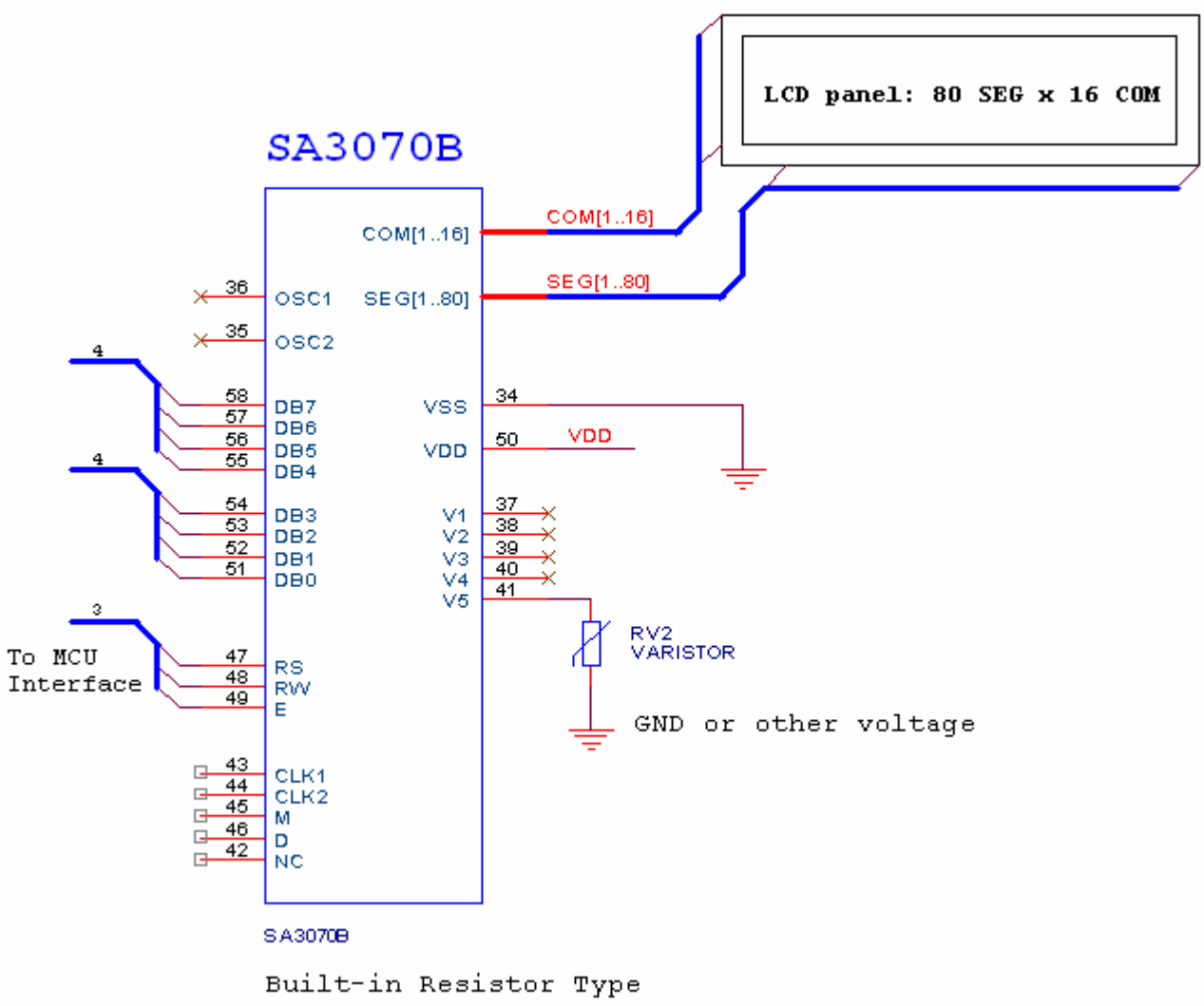


Figure 28. Read Mode Timing Diagram

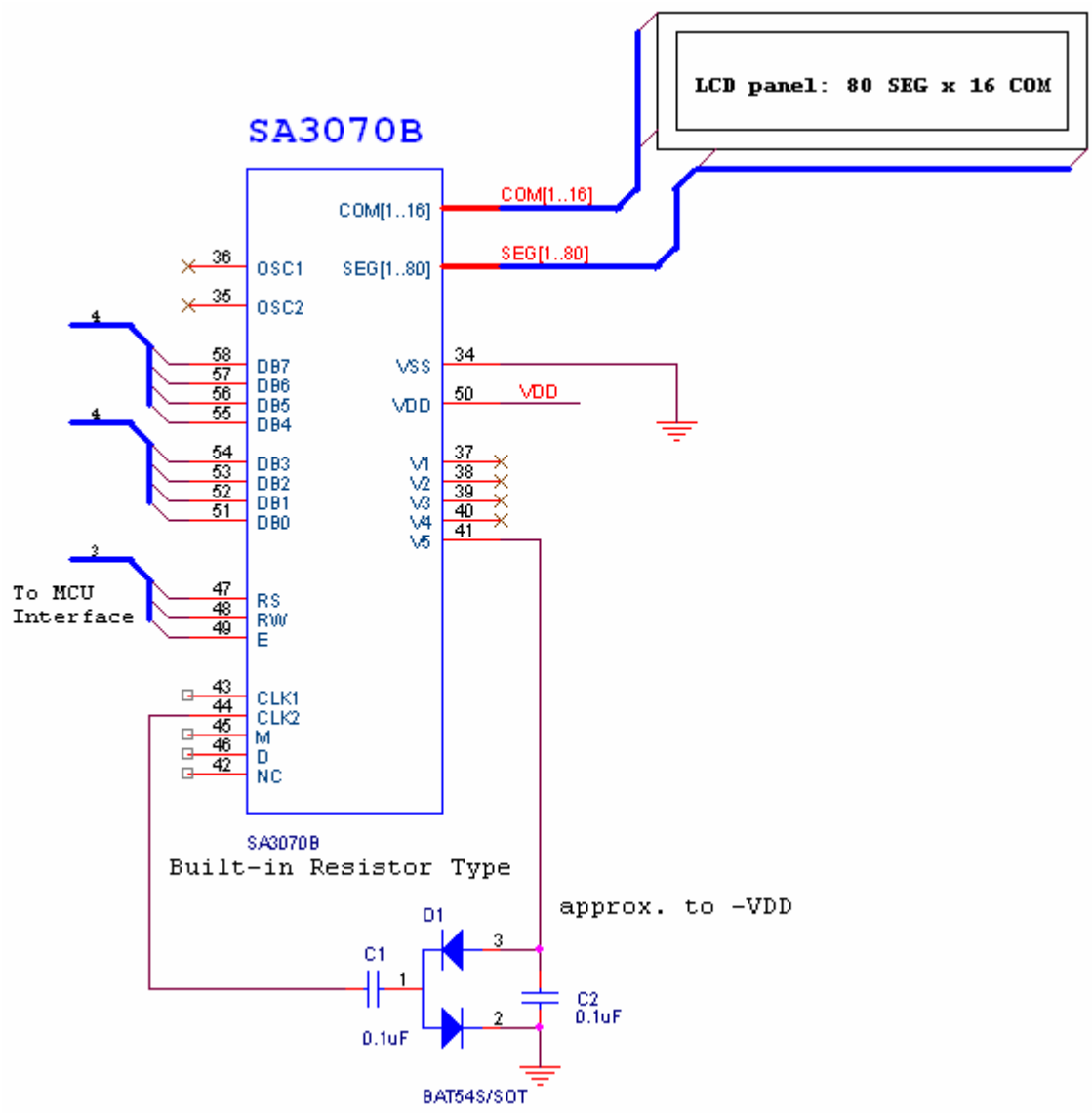
12. Application Information of SA3070B



Substrate should be connected VDD or floating and use 1 mil bonding wire

Recommend: The operation voltage of LCD is about 4.5 to 5V

13. Application Information of SA3070B



Substrate should be connected VDD or floating and use 1 mil bonding wire

Recommend: The operation voltage of LCD is about 4.5 to 5V

If VDD = 3.0V, BAT54S could provide a negative voltage in approximate to 80% efficiency and forward bias voltage between pin 1 and 3 = ~0.4V.

Therefore, V5 = -0.8 * 3.0V + 0.4= -2.0V

Such that VLCD = VDD – V5 = ~5.0V

CGROM Pattern

SA3070B-01 pattern.