■ DESCRIPTION

The RW1020 families of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The drivers are available in two configurations
The RW1020 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.
These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

- The RW1020 which is able to drive two lines of twelve characters each.
- The RW1021 which is able to drive 80 segments for extension.
- The RW1022 which is able to drive one line of thirteen characters each.
- 0A/AA mode select by pin without extra PCB layout
- SED1520 series compatible

■ FEATURES

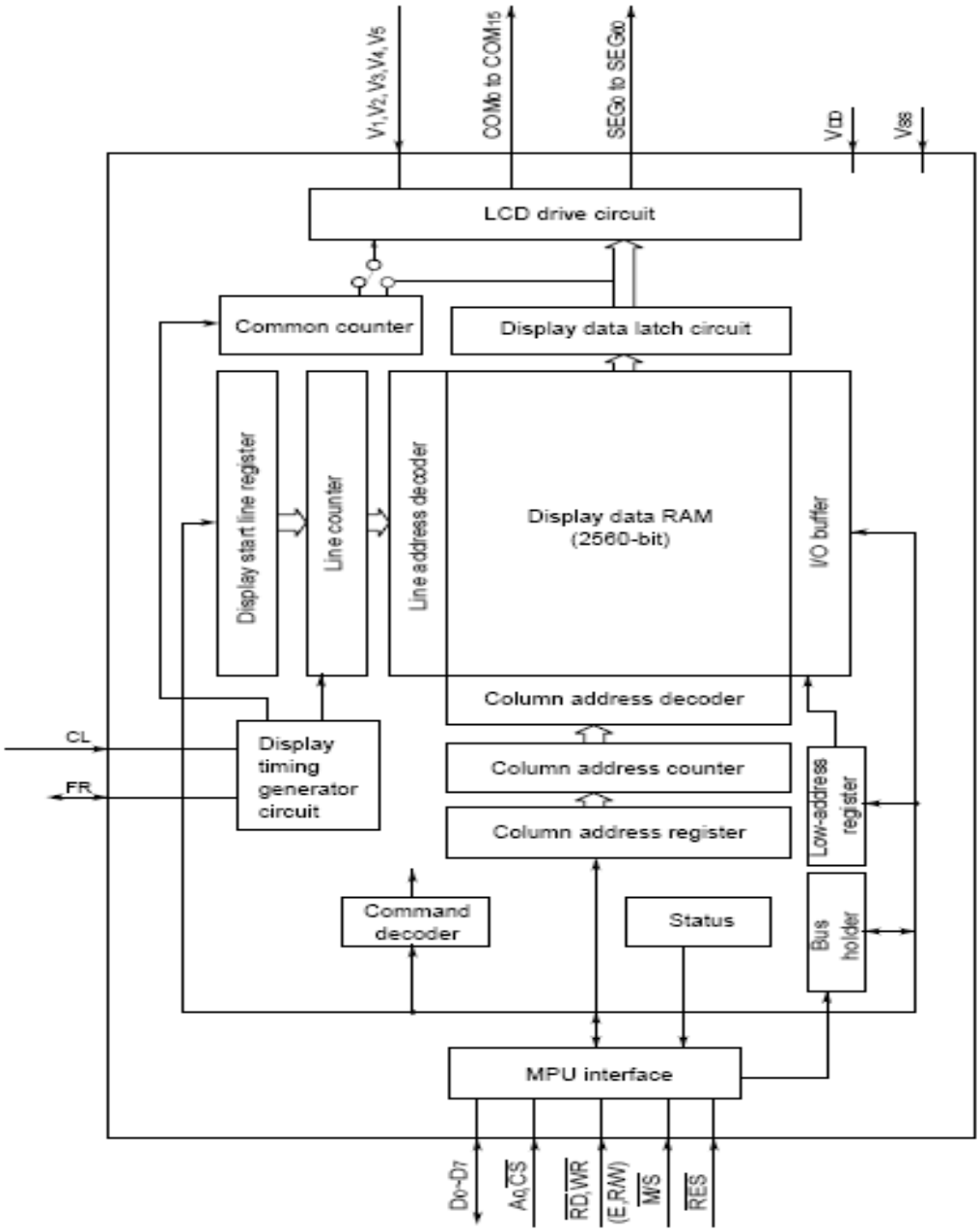
- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Many command set
- Total 80 (segment + common) drive sets
- Low power — 30 μW at 2 kHz external clock
- Wide range of supply voltages
  V_{DD} – V_{SS}: –2.4 to 5.5 V
  V_{DD} – V_5: –3.5 to –7.0 V
- Low-power CMOS

■ LINE-UP

Product Name	Clock Frequency		Applicable Driver	Number of SEG Drivers	Number of COM Drivers	Duty
	On-chip	External				
RW1020*0*	18 KHz	18 KHz	RW1020*0*, RW1021*0*	61	16	1/16 , 1/32
RW1021*0*	-	18 KHz	RW1020*0*, RW1022*0*	80	0	1/8 to 1/32
RW1022*0*	18 KHz	18 KHz	RW1022*0*, RW1021*0*	69	8	1/8 , 1/16
RW1020*A*	-	2 KHz	RW1020*A*, RW1021*A*	61	16	1/16 , 1/32
RW1021*A*	-	2 KHz	RW1020*A*, RW1022*A*	80	0	1/8 to 1/32
RW1022*A*	-	2 KHz	RW1022*A*, RW1021*A*	69	8	1/8 , 1/16

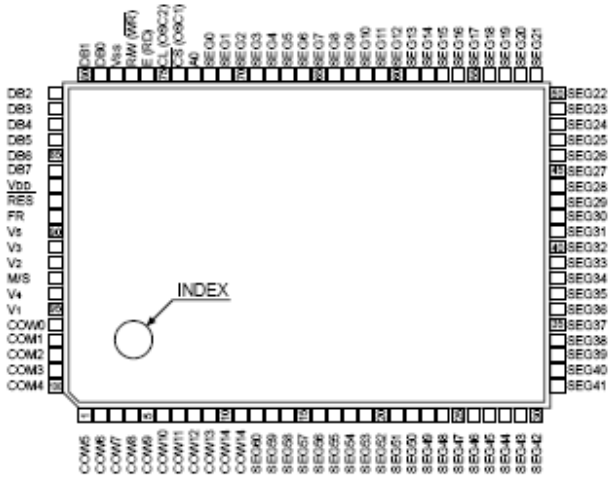
RW1020 Specification Revision History		
Version	**Date**	**Description**
1.0	2007/1/29	Add AC Characteristics
1.1	2007/2/9	Add RW1020*0A and RW1020*AA stander circuit
1.2	2007/2/9	Revise DC spec
1.3	2007/4/9	Add RW1021*0* Pad Center coordinates

■ BLOCK DIAGRAM

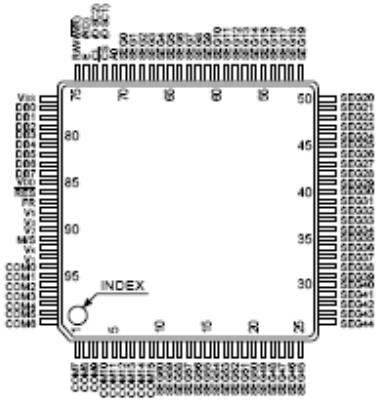


■ PACKAGE CONFIGURATION

QFP5-100pin



QFP15-100pin



Note: This is an example of RW1020F pin assignment. The modified pin names are given below.

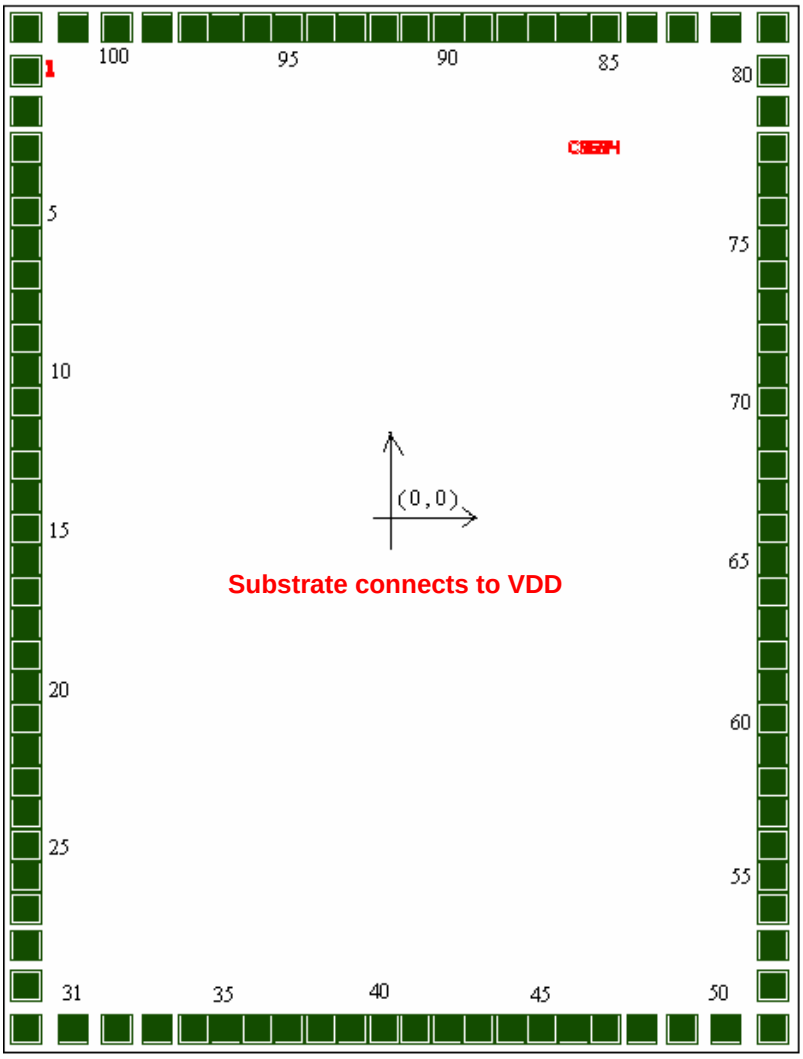
Product Name	Pin/Pad Number					
	74	75	98 to 102, 1 to 11	93	94	95
RW1020F0A	OSC1	OSC2	COM0 to COM15	M/S	V4	V1
RW1021F0A	$\overline{CS}$	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
RW1022F0A	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V4	V1
RW1020FAA	$\overline{CS}$	CL	COM0 to COM15	M/S	V4	V1
RW1021FAA	$\overline{CS}$	CL	SEG76 to SEG72, SEG71 to SEG61	SEG79	SEG78	SEG77
RW1022FAA	$\overline{CS}$	CL	COM0 to 7, SEG68 to 61	M/S	V4	V1

RW1020: Common outputs COM0 to COM15 of the master LSI correspond to COM31 to COM16 of the slave LSI.
RW1022: Common outputs COM0 to COM15 of the master LSI correspond to COM15 to COM8 of the slave LSI.

■ PAD LAYOUT

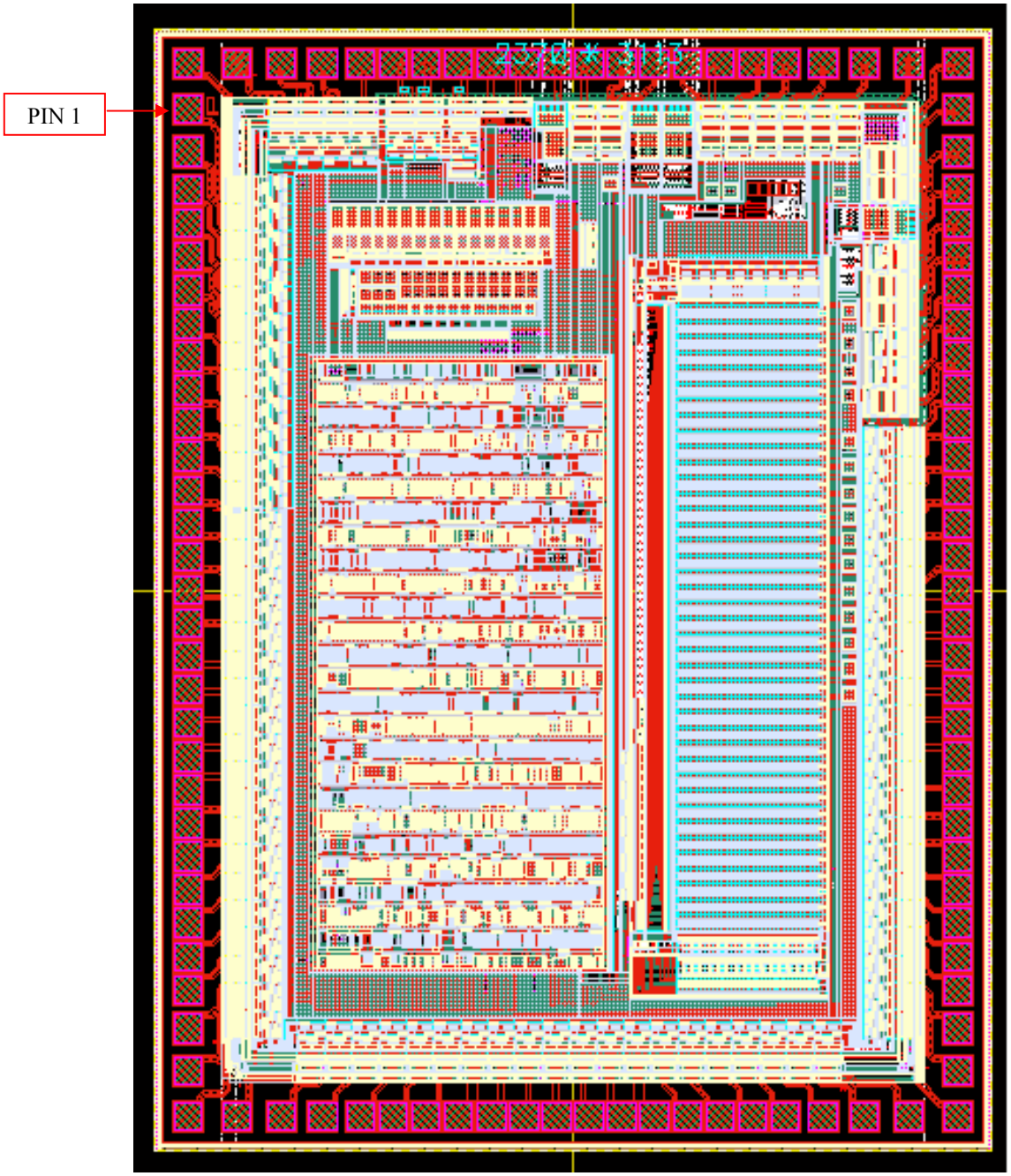
Chip specifications of AL pad package

Chip size: 2370um x 3113um
Pad pitch: 92.5um ~ 127.5um
Pad Size: 87.5um x 87.5um



Note: An example of RW1020*AA die numbers is given. These numbers are the same as the bump package

■ CHIP LAYOUT



■ PAD ARRANGEMENT

An example of RW1020*A* pin names is given. The asterisk (*) can be A for AL pad package or B for gold bump package.

RW1020*AA Pad Center Coordinates

Pad No	Pin Name	X	Y	Pad No	Pin Name	X	Y	Pad No	Pin Name	X	Y
1	COM5	-1091.3	1335.3	35	SEG37	-508.8	-1462.8	69	SEG3	1091.3	277.8
2	COM6	-1091.3	1217.8	36	SEG36	-416.3	-1462.8	70	SEG2	1091.3	370.3
3	COM7	-1091.3	1110.3	37	SEG35	-323.8	-1462.8	71	SEG1	1091.3	462.8
4	COM8	-1091.3	1017.8	38	SEG34	-231.3	-1462.8	72	SEG0	1091.3	555.3
5	COM9	-1091.3	925.3	39	SEG33	-138.8	-1462.8	73	A0	1091.3	647.8
6	COM10	-1091.3	832.8	40	SEG32	-46.3	-1462.8	74	$\overline{CS}$	1091.3	740.3
7	COM11	-1091.3	740.3	41	SEG31	46.3	-1462.8	75	CL	1091.3	832.8
8	COM12	-1091.3	647.8	42	SEG30	138.8	-1462.8	76	E($\overline{RD}$)	1091.3	925.3
9	COM13	-1091.3	555.3	43	SEG29	231.3	-1462.8	77	R/W($\overline{WR}$)	1091.3	1017.8
10	COM14	-1091.3	462.8	44	SEG28	323.8	-1462.8	78	MODEP	1091.3	1110.3
11	COM15	-1091.3	370.3	45	SEG27	416.3	-1462.8	79	VSS	1091.3	1217.8
12	SEG60	-1091.3	277.8	46	SEG26	508.8	-1462.8	80	DB0	1091.3	1335.3
13	SEG59	-1091.3	185.3	47	SEG25	601.3	-1462.8	81	DB1	1091.3	1462.8
14	SEG58	-1091.3	92.8	48	SEG24	708.8	-1462.8	82	DB2	953.8	1462.8
15	SEG57	-1091.3	0.3	49	SEG23	826.3	-1462.8	83	DB3	826.3	1462.8
16	SEG56	-1091.3	-92.3	50	SEG22	953.8	-1462.8	84	DB4	708.8	1462.8
17	SEG55	-1091.3	-184.8	51	SEG21	1091.3	-1462.8	85	DB5	601.3	1462.8
18	SEG54	-1091.3	-277.3	52	SEG20	1091.3	-1335.3	86	DB6	508.8	1462.8
19	SEG53	-1091.3	-369.8	53	SEG19	1091.3	-1217.8	87	DB7	416.3	1462.8
20	SEG52	-1091.3	-462.3	54	SEG18	1091.3	-1110.3	88	VDD	323.8	1462.8
21	SEG51	-1091.3	-554.8	55	SEG17	1091.3	-1017.3	89	VDD	231.3	1462.8
22	SEG50	-1091.3	-647.3	56	SEG16	1091.3	-924.8	90	$\overline{RES}$	138.8	1462.8
23	SEG49	-1091.3	-739.8	57	SEG15	1091.3	-832.3	91	FR	46.3	1462.8
24	SEG48	-1091.3	-832.3	58	SEG14	1091.3	-739.8	92	V5	-46.3	1462.8
25	SEG47	-1091.3	-924.8	59	SEG13	1091.3	-647.3	93	V3	-138.8	1462.8
26	SEG46	-1091.3	-1017.3	60	SEG12	1091.3	-554.8	94	V2	-231.3	1462.8
27	SEG45	-1091.3	-1110.3	61	SEG11	1091.3	-462.3	95	M/S	-323.8	1462.8
28	SEG44	-1091.3	-1217.8	62	SEG10	1091.3	-369.8	96	V4	-416.3	1462.8
29	SEG43	-1091.3	-1335.3	63	SEG9	1091.3	-277.3	97	V1	-508.8	1462.8
30	SEG42	-1091.3	-1462.8	64	SEG8	1091.3	-184.8	98	COM0	-601.3	1462.8
31	SEG41	-953.8	-1462.8	65	SEG7	1091.3	-92.3	99	COM1	-708.8	1462.8
32	SEG40	-826.3	-1462.8	66	SEG6	1091.3	0.3	100	COM2	-826.3	1462.8
33	SEG39	-708.8	-1462.8	67	SEG5	1091.3	92.8	101	COM3	-953.8	1462.8
34	SEG38	-601.3	-1462.8	68	SEG4	1091.3	185.3	102	COM4	-1091.3	1462.8

- **PAD 88, 89 are connected together inside the IC.**

RW1020*0A Pad Center Coordinates

Pad No	Pin Name	X	Y	Pad No	Pin Name	X	Y	Pad No	Pin Name	X	Y
1	COM5	-1091.3	1335.3	35	SEG37	-508.8	-1462.8	69	SEG3	1091.3	277.8
2	COM6	-1091.3	1217.8	36	SEG36	-416.3	-1462.8	70	SEG2	1091.3	370.3
3	COM7	-1091.3	1110.3	37	SEG35	-323.8	-1462.8	71	SEG1	1091.3	462.8
4	COM8	-1091.3	1017.8	38	SEG34	-231.3	-1462.8	72	SEG0	1091.3	555.3
5	COM9	-1091.3	925.3	39	SEG33	-138.8	-1462.8	73	A0	1091.3	647.8
6	COM10	-1091.3	832.8	40	SEG32	-46.3	-1462.8	74	OSC1	1091.3	740.3
7	COM11	-1091.3	740.3	41	SEG31	46.3	-1462.8	75	OSC2	1091.3	832.8
8	COM12	-1091.3	647.8	42	SEG30	138.8	-1462.8	76	E($\overline{RD}$)	1091.3	925.3
9	COM13	-1091.3	555.3	43	SEG29	231.3	-1462.8	77	R/W($\overline{WR}$)	1091.3	1017.8
10	COM14	-1091.3	462.8	44	SEG28	323.8	-1462.8	78	MODEP	1091.3	1110.3
11	COM15	-1091.3	370.3	45	SEG27	416.3	-1462.8	79	VSS	1091.3	1217.8
12	SEG60	-1091.3	277.8	46	SEG26	508.8	-1462.8	80	DB0	1091.3	1335.3
13	SEG59	-1091.3	185.3	47	SEG25	601.3	-1462.8	81	DB1	1091.3	1462.8
14	SEG58	-1091.3	92.8	48	SEG24	708.8	-1462.8	82	DB2	953.8	1462.8
15	SEG57	-1091.3	0.3	49	SEG23	826.3	-1462.8	83	DB3	826.3	1462.8
16	SEG56	-1091.3	-92.3	50	SEG22	953.8	-1462.8	84	DB4	708.8	1462.8
17	SEG55	-1091.3	-184.8	51	SEG21	1091.3	-1462.8	85	DB5	601.3	1462.8
18	SEG54	-1091.3	-277.3	52	SEG20	1091.3	-1335.3	86	DB6	508.8	1462.8
19	SEG53	-1091.3	-369.8	53	SEG19	1091.3	-1217.8	87	DB7	416.3	1462.8
20	SEG52	-1091.3	-462.3	54	SEG18	1091.3	-1110.3	88	VDD	323.8	1462.8
21	SEG51	-1091.3	-554.8	55	SEG17	1091.3	-1017.3	89	VDD	231.3	1462.8
22	SEG50	-1091.3	-647.3	56	SEG16	1091.3	-924.8	90	$\overline{RES}$	138.8	1462.8
23	SEG49	-1091.3	-739.8	57	SEG15	1091.3	-832.3	91	FR	46.3	1462.8
24	SEG48	-1091.3	-832.3	58	SEG14	1091.3	-739.8	92	V5	-46.3	1462.8
25	SEG47	-1091.3	-924.8	59	SEG13	1091.3	-647.3	93	V3	-138.8	1462.8
26	SEG46	-1091.3	-1017.3	60	SEG12	1091.3	-554.8	94	V2	-231.3	1462.8
27	SEG45	-1091.3	-1110.3	61	SEG11	1091.3	-462.3	95	M/S	-323.8	1462.8
28	SEG44	-1091.3	-1217.8	62	SEG10	1091.3	-369.8	96	V4	-416.3	1462.8
29	SEG43	-1091.3	-1335.3	63	SEG9	1091.3	-277.3	97	V1	-508.8	1462.8
30	SEG42	-1091.3	-1462.8	64	SEG8	1091.3	-184.8	98	COM0	-601.3	1462.8
31	SEG41	-953.8	-1462.8	65	SEG7	1091.3	-92.3	99	COM1	-708.8	1462.8
32	SEG40	-826.3	-1462.8	66	SEG6	1091.3	0.3	100	COM2	-826.3	1462.8
33	SEG39	-708.8	-1462.8	67	SEG5	1091.3	92.8	101	COM3	-953.8	1462.8
34	SEG38	-601.3	-1462.8	68	SEG4	1091.3	185.3	102	COM4	-1091.3	1462.8

The other RW1020 series packages have the different pin names as shown.

- **PAD 88, 89 are connected together inside the IC.**

RW1021*0* Pad Center Coordinates

Pad No	Pin Name	X	Y	Pad No	Pin Name	X	Y	Pad No	Pin Name	X	Y
1	SEG71	-1091.3	1335.3	35	SEG37	-508.8	-1462.8	69	SEG3	1091.3	277.8
2	SEG70	-1091.3	1217.8	36	SEG36	-416.3	-1462.8	70	SEG2	1091.3	370.3
3	SEG69	-1091.3	1110.3	37	SEG35	-323.8	-1462.8	71	SEG1	1091.3	462.8
4	SEG68	-1091.3	1017.8	38	SEG34	-231.3	-1462.8	72	SEG0	1091.3	555.3
5	SEG67	-1091.3	925.3	39	SEG33	-138.8	-1462.8	73	A0	1091.3	647.8
6	SEG66	-1091.3	832.8	40	SEG32	-46.3	-1462.8	74	OSC1	1091.3	740.3
7	SEG65	-1091.3	740.3	41	SEG31	46.3	-1462.8	75	OSC2	1091.3	832.8
8	SEG64	-1091.3	647.8	42	SEG30	138.8	-1462.8	76	E($\overline{RD}$)	1091.3	925.3
9	SEG63	-1091.3	555.3	43	SEG29	231.3	-1462.8	77	R/W($\overline{WR}$)	1091.3	1017.8
10	SEG62	-1091.3	462.8	44	SEG28	323.8	-1462.8	78	MODEP	1091.3	1110.3
11	SEG61	-1091.3	370.3	45	SEG27	416.3	-1462.8	79	VSS	1091.3	1217.8
12	SEG60	-1091.3	277.8	46	SEG26	508.8	-1462.8	80	DB0	1091.3	1335.3
13	SEG59	-1091.3	185.3	47	SEG25	601.3	-1462.8	81	DB1	1091.3	1462.8
14	SEG58	-1091.3	92.8	48	SEG24	708.8	-1462.8	82	DB2	953.8	1462.8
15	SEG57	-1091.3	0.3	49	SEG23	826.3	-1462.8	83	DB3	826.3	1462.8
16	SEG56	-1091.3	-92.3	50	SEG22	953.8	-1462.8	84	DB4	708.8	1462.8
17	SEG55	-1091.3	-184.8	51	SEG21	1091.3	-1462.8	85	DB5	601.3	1462.8
18	SEG54	-1091.3	-277.3	52	SEG20	1091.3	-1335.3	86	DB6	508.8	1462.8
19	SEG53	-1091.3	-369.8	53	SEG19	1091.3	-1217.8	87	DB7	416.3	1462.8
20	SEG52	-1091.3	-462.3	54	SEG18	1091.3	-1110.3	88	VDD	323.8	1462.8
21	SEG51	-1091.3	-554.8	55	SEG17	1091.3	-1017.3	89	VDD	231.3	1462.8
22	SEG50	-1091.3	-647.3	56	SEG16	1091.3	-924.8	90	$\overline{RES}$	138.8	1462.8
23	SEG49	-1091.3	-739.8	57	SEG15	1091.3	-832.3	91	FR	46.3	1462.8
24	SEG48	-1091.3	-832.3	58	SEG14	1091.3	-739.8	92	V5	-46.3	1462.8
25	SEG47	-1091.3	-924.8	59	SEG13	1091.3	-647.3	93	V3	-138.8	1462.8
26	SEG46	-1091.3	-1017.3	60	SEG12	1091.3	-554.8	94	V2	-231.3	1462.8
27	SEG45	-1091.3	-1110.3	61	SEG11	1091.3	-462.3	95	SEG79	-323.8	1462.8
28	SEG44	-1091.3	-1217.8	62	SEG10	1091.3	-369.8	96	SEG78	-416.3	1462.8
29	SEG43	-1091.3	-1335.3	63	SEG9	1091.3	-277.3	97	SEG77	-508.8	1462.8
30	SEG42	-1091.3	-1462.8	64	SEG8	1091.3	-184.8	98	SEG76	-601.3	1462.8
31	SEG41	-953.8	-1462.8	65	SEG7	1091.3	-92.3	99	SEG75	-708.8	1462.8
32	SEG40	-826.3	-1462.8	66	SEG6	1091.3	0.3	100	SEG74	-826.3	1462.8
33	SEG39	-708.8	-1462.8	67	SEG5	1091.3	92.8	101	SEG73	-953.8	1462.8
34	SEG38	-601.3	-1462.8	68	SEG4	1091.3	185.3	102	SEG72	-1091.3	1462.8

Product Name	Pin/Pad Number					
	74	75	98 to 102, 1 to 11	95	96	97
RW1022*0*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V4	V1
RW1022*A*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V4	V1
RW1021*0*	CSB	CL	SEG76 to SEG72, SEG71 to SEG61,	SEG79	SEG78	SEG77
RW1022*A*	CSB	CL	SEG76 to SEG61	SEG79	SEG78	SEG77

■ PIN DESCRIPTION

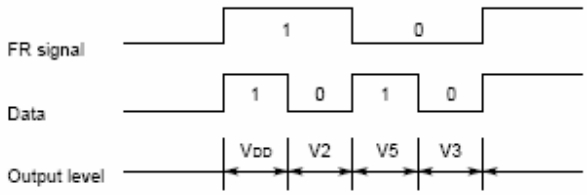
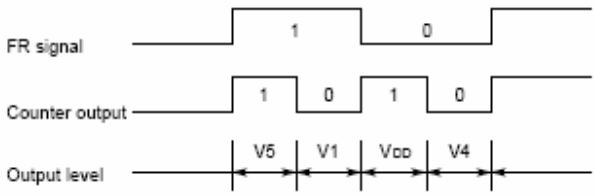
(1) Power Pins

Name	Description
V_{DD}	Connected to the +5Vdc power. Common to the V_{CC} MPU power pin.
V_{SS}	0 Vdc pin connected to the system ground.
V_1, V_2, V_3, V_4, V_5	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$

(2) System Bus Connection Pins

D7 to D0	Three-state I/O. The 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0: D0 to D7 are display control data. A0=1: D0 to D7 are display data.
$\overline{RES}$	Input. When the $\overline{RES}$ signal goes ⌐└⌐ the 68-series MPU is initialized, and when it goes _┌┘_ , the 80-series MPU is initialized. The system is reset during edge sense of the $\overline{RES}$ signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows: High level: 68-series MPU interface Low level: 80-series MPU interface
$\overline{CS}$	Input. Active low. Effective for an external clock operation model only. An address bus signal is usually decoded by use of chip select signal, and it is entered. If the system has a built-in oscillator, this is used as an input pin to the oscillator amp and an Rf oscillator resistor is connected to it. In such case, the $\overline{RD}$, $\overline{WR}$ and E signals must be ORed with the $\overline{CS}$ signals and entered.
E ($\overline{RD}$)	• If the 68-series MPU is connected: Input. Active high. Used as an enable clock input of the 68-series MPU. • If the 80-series MPU is connected: Input. Active low. The $\overline{RD}$ signal of the 80-series MPU is entered in this pin. When this signal is kept low, the SED1520 data bus is in the output status.
R/W ($\overline{WR}$)	• If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is high) or write control signals (if low). • If the 80-series MPU is connected: Input. Active low. The $\overline{WR}$ signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of $\overline{WR}$ signal.

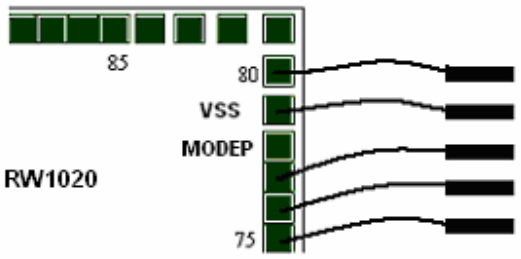
(3) LCD Drive Circuit Signals

Name	Description
CL	Input. Effective for an external clock operation model only. This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges. If the system has a built-in oscillator, this is used as an output pin of the oscillator amp and an Rf oscillator resistor is connected to it.
FR	Input/output. This is an I/P pin of LCD AC signals, and connected to the M terminal of common driver. I/O selection • Common oscillator built-in model: Output if M/S is 1; Input if M/S is 0. • Dedicate segment model: Input
SEGn	Output. The output pin for LCD column (segment) driving. A single level of V_{DD}, V_2, V_3 and V_5 is selected by the combination of display RAM contents and RF signal. 
COMn	Output. The output pin for LCD common (low) driving. A single level of V_{DD}, V_1, V_4 and V_5 is selected by the combination of common counter output and RF signal. The slave LSI has the reverse common output scan sequence than the master LSI. 

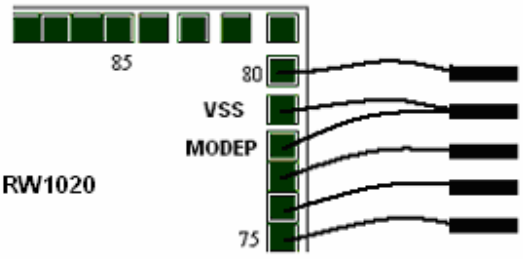
<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>M/S</td><td>Input.
The master or slave LSI operation select pin for the RW1020 or RW1022
Connected to VDD (to select the master LSI operation mode) or Vss (to select the slave LSI operation mode).
When this M/S pin is set, the functions of FR, COM0 to COM15, OSC1 (CS), and OSC2 (CL) pins are changed.
<table>
<tr><th></th><th>M/S</th><th>FR</th><th>COM output</th><th>OSC1</th><th>OSC2</th></tr>
<tr><td rowspan="2">RW1020F0A</td><td>VDD</td><td>Output</td><td>COM0 to COM15</td><td>Input</td><td>Output</td></tr>
<tr><td>Vss</td><td>Input</td><td>COM31 to COM16</td><td>NC</td><td>Input</td></tr>
<tr><td rowspan="2">RW1022F0A</td><td>VDD</td><td>Output</td><td>COM0 to COM7</td><td>Input</td><td>Output</td></tr>
<tr><td>Vss</td><td>Input</td><td>COM15 to COM8</td><td>NC</td><td>Input</td></tr>
</table>
* The slave driver has the reverse common output scan sequence than the master driver.</td></tr>
<tr><td>MODEP</td><td>* AA Mode (external clock) : Keep this pin open
* 0A MOde (on-chip RC oscillation) : bonding this pin to VSS level

Mode select pin with pull-up resistor
<table>
<tr><th></th><th>Product Name</th><th colspan="2">Clock Frequency</th></tr>
<tr><th></th><th></th><th>MS=1</th><th>MS=0</th></tr>
<tr><th></th><th></th><th>On-chip for Master</th><th>External for Slave</th></tr>
<tr><td rowspan="3">MODEP= 0</td><td>RW1020*0*</td><td>18 KHz</td><td>18 KHz</td></tr>
<tr><td>RW1021*0*</td><td>-</td><td>18 KHz</td></tr>
<tr><td>RW1022*0*</td><td>18 KHz</td><td>18 KHz</td></tr>
<tr><td rowspan="3">MODEP= 1</td><td>RW1020*A*</td><td>-</td><td>2 KHz</td></tr>
<tr><td>RW1021*A*</td><td>-</td><td>2 KHz</td></tr>
<tr><td>RW1022*A*</td><td>-</td><td>2 KHz</td></tr>
</table></td></tr>
</table>

'AA MODE(External clock) : MODEP pin keep open



'0A MODE(Internal CR oscillation) : MODEP bonding to VSS



■ BLOCK DESCRIPTION

System Bus

➢ **MPU interface**

1. Selecting an interface type

The RW1020 series transfers data via 8-bit bidirectional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of high or low $\overline{RES}$ signal level after reset (see Table 1).

When the $\overline{CS}$ signal is high, the RW1020 series is disconnected from the MPU bus and set to stand by. However, the reset signal is entered regardless of the internal setup status.

Table 1

$\overline{RES}$ signal input level	MPU type	A0	E	R/W	CS	D0 to D7
Active low	68-series	↑	↑	↑	↑	↑
Active high	80-series	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

➢ **Data transfer**

The RW1020 and RW1021 drivers use the A0, E (or $\overline{RD}$) and R/W (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table blow.

In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RFAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1. No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

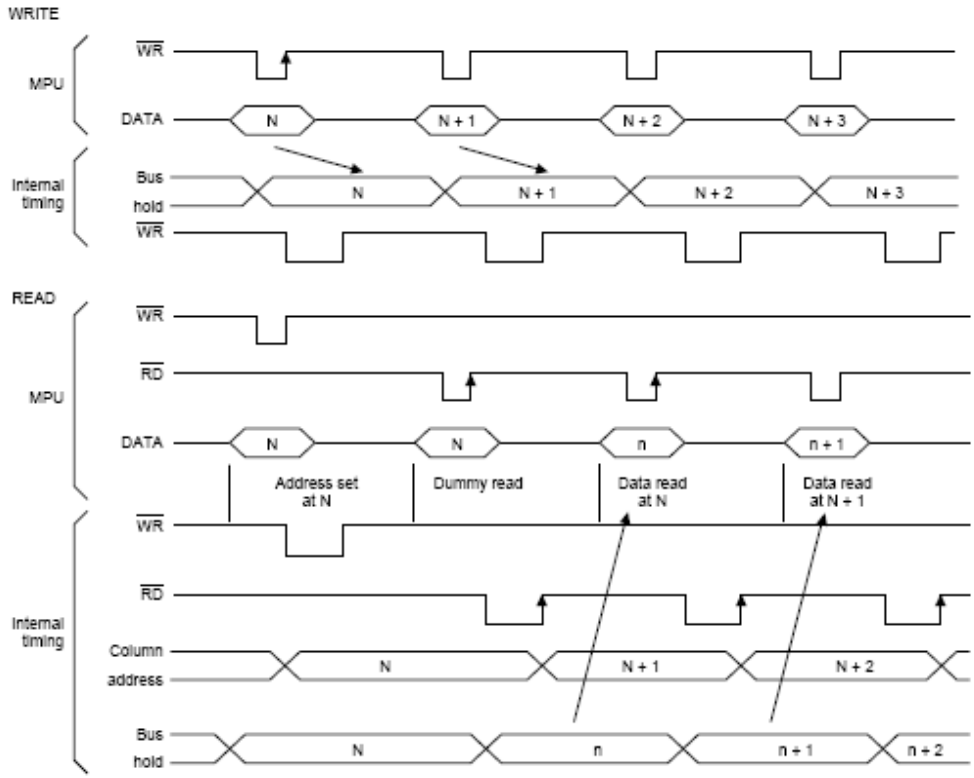


Figure 1 Bus Buffer Delay

➢ Busy flag

When the Busy flag is logical 1, the RW1020 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

➢ Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. See section 3.
The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits

➢ Column Address Counter

The column address counter is a 7-bit pre-settable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

➢ Page Register

The page register is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 2. The contents of the page register are set by the Set Page Register command.

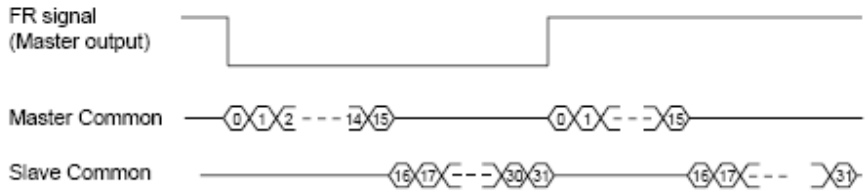
➢ Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 2 .

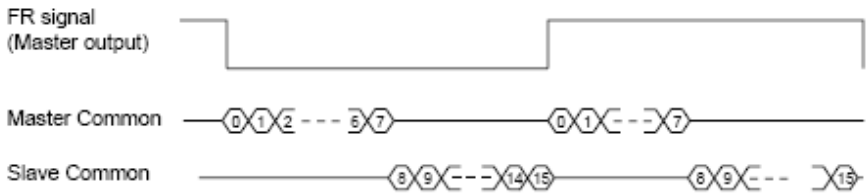
■ Common Timing Generator Circuit

Generates common timing signals and FR frame signals from the CL basic clock. The 1/16 or 1/32 duty (for RW1020) or 1/8 or 1/16 duty (for RW1022) can be selected by the Duty Select command. If the 1/32 duty is selected for the RW1020 and 1/16 duty is selected for the RW1022, the 1/32 and 1/16 duties are provided by two chips consisting of the master and slave chips in the common multi-chip mode.

RW1020



RW1022



➢ Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF and Static Drive ON/OFF commands.

➢ LCD Driver Circuit

The LCD driver circuitry generates the 80 4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

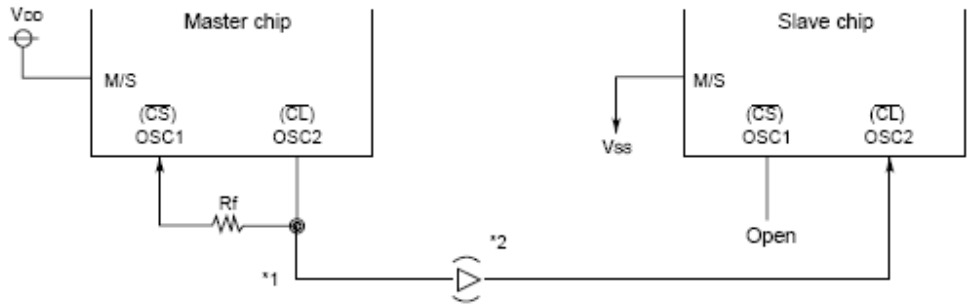
➢ Display Timing Generator

This circuit generates the internal display timing signal using the basic clock, CL, and the frame signals, FR.
FR is used to generate the dual frame AC-drive waveform
(type B drive) and to lock the line counter and common timing generator to the system frame rate.
CL is used to lock the line counter to the system line scan rate. If a system uses both RW1020s or RW1022 and RW1021s they must have the same CL frequency rating.

■ Oscillator Circuit (RW1020*0A Only)

A low power-consumption CR oscillator for adjusting the oscillation frequency using Rf oscillation resistor only. This circuit generates a display timing signal. Some of RW1020 and RW1022 series models have a built-in oscillator and others use an external clock. This difference must be checked before use.
Connect the Rf oscillation resistor as follows. To suppress the built-in oscillator circuit and drive the MPU using an external clock, enter the clock having the same phase as the OSC2 of mater chip into OSC2 of the slave chip.

• MPU having a built-in oscillator



*1 If the parasitic capacitance of this section increases, the oscillation frequency may shift to the lower frequency. Therefore, the Rf oscillation frequency must be reduced below the specified level.
*2 A CMOS buffer is required if the oscillation circuit is connected to two or more slave MPU chips.

• MPU driven with an external clock

■ Reset Circuit

Detects a rising or falling edge of an $\overline{RES}$ input and initializes the MPU during power-on.
• Initialization status
1. Display is off.
2. Display start line register is set to line 1.
3. Static drive is turned off.
4. Column address counter is set to address 0.
5. Page address register is set to page 3.
6. 1/32 duty (RW1020) or 1/16 duty (RW1022) is selected.
7. Forward ADC is selected (ADC command D0 is 1 and ADC status flag is 1).
8. Read-modify-write is turned off.

The input signal level at pin is sensed, and an MPU interface mode is selected as shown on Table 1.
For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.
As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.
If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur.
When the Reset command is issued, initialization

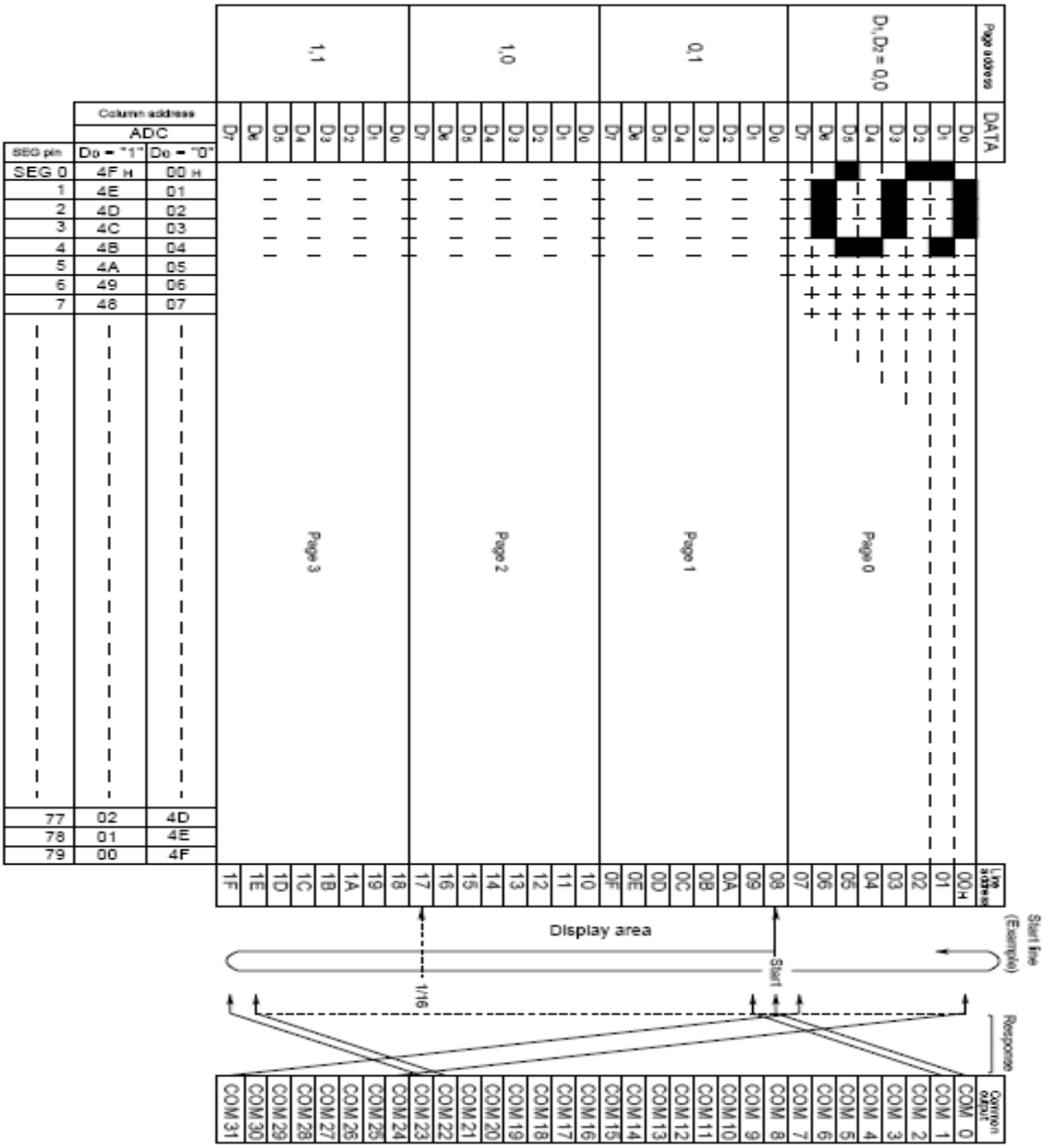


Figure 2 Display data RAM Addressing

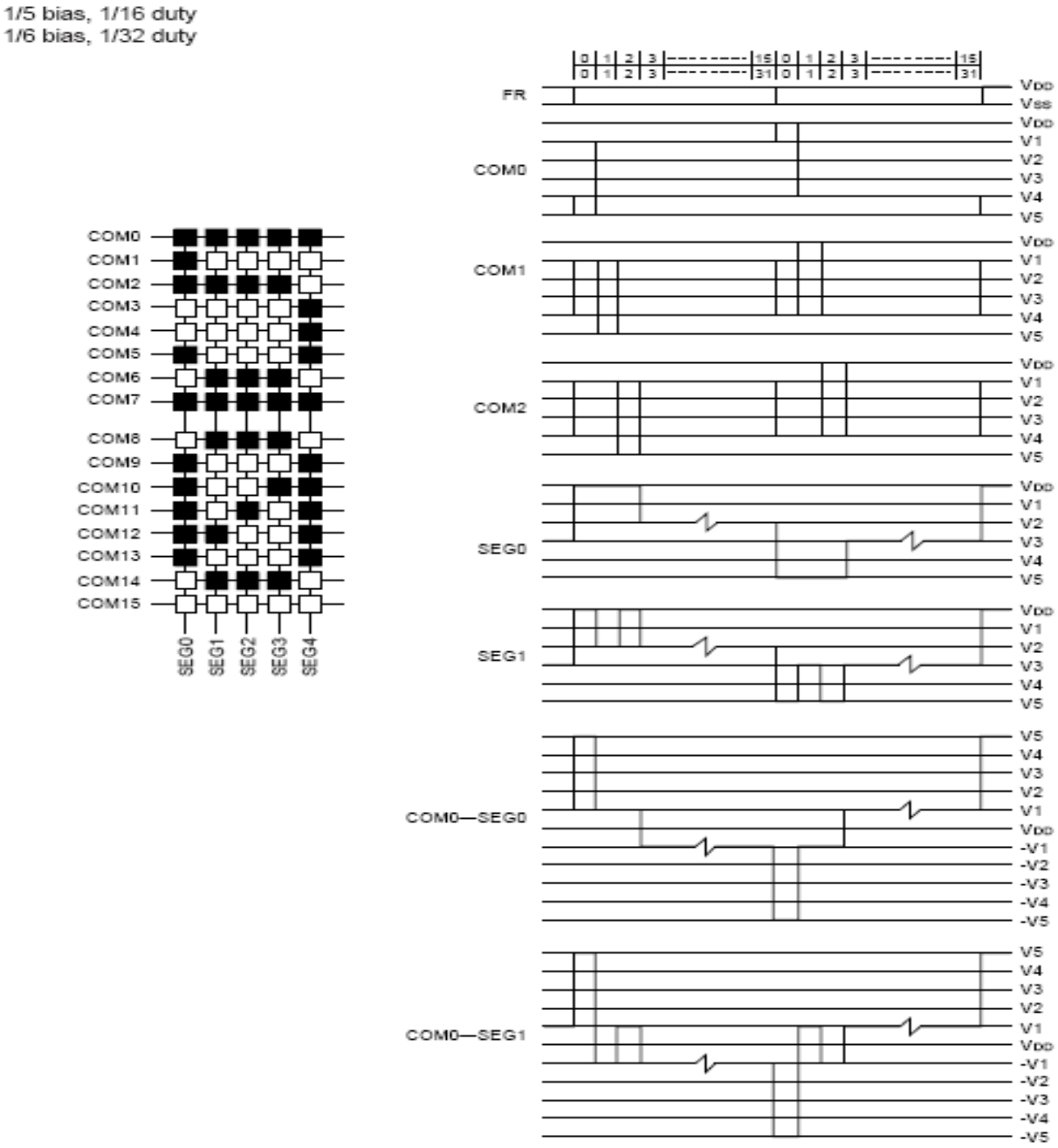


Figure 4 LCD drive waveforms example

■ COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1: CCW output
Statis drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1: 1/32, 0: 1/16
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Table3. Command table

■ Command Description

Table 3 is the command table. The RW1020 series identifies a data bus using a combination of A0 and R/W ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

➢ Display ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.
• D=1: Display ON
• D=0: Display OFF

➢ Display Start Line

This command specifies the line address shown in Figure 3 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	0	A4	A3	A2	A1	A0	C0H to DFH

This command loads the display start line register.

See Figure 2.

➢ Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	1	0	A1	A0	B8H to BBH

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

➢ **Set Column Address**

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	A6	A5	A4	A3	A2	A1	A0	00H to 4FH

This command loads the column address register.

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			⋮				⋮
1	0	0	1	1	1	1	79

➢ **Read Status**

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

• The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
• The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column addresses n → segment driver n.
  ADC=0: Inverted. Column addresses 79-u → segment driver u.
• The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
• The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

➢ **Write Display Data**

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

➢ **Read Display Data**

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

➢ **Select ADC**

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH … (inverted)
D=0: SEG0 ← column address 00H … (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

➢ **Static Drive ON/OFF**

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

➢ **Select Duty**

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the RW1020F and RW1022F. It is invalid for the RW1021F which performs passive operation. The duty cycle of the RW1021F is determined by the externally generated FR signal.

	RW1020	RW1022
D=1:	1/32 duty cycle	1/16 duty cycle
D=0:	1/16 duty cycle	1/8 duty cycle

When using the RW1020F0A, RW1022F0A (having a built-in oscillator) and the RW1021F0A continuously, set the duty as follows:

		RW1021F0A
RW1020F0A	1/32	1/32
	1/16	1/16
RW1022F0A	1/16	1/32
	1/8	1/16

➢ **Read-Modify-Write**

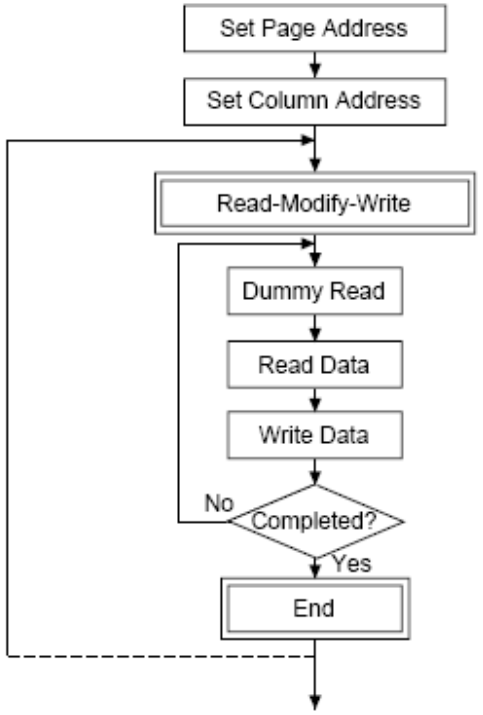
A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an End command is received.

• Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

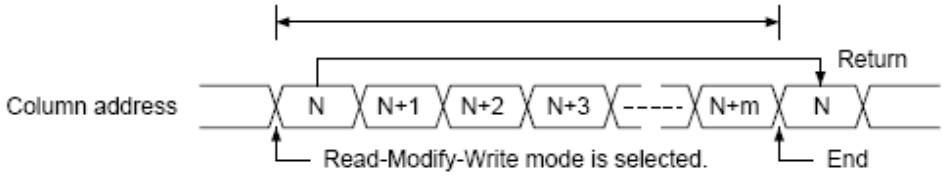
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



➢ **End**

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



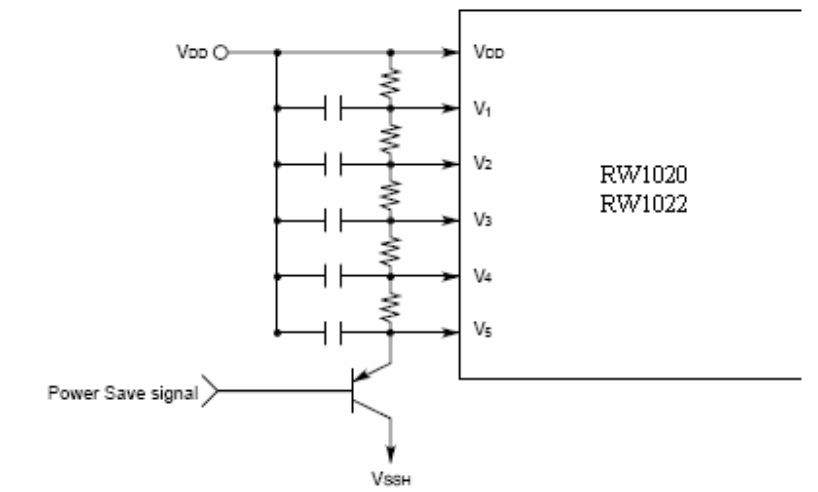
➢ **Reset**

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears
• the display start line register.
• and set page address register to 3 page.
It does not affect the contents of the display data RAM.
When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

■ Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the VDD level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is related when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



If the LCD drive power is generated by resistance division, the resistance and capacitance are determined by the LCD panel size. After the panel size has been determined, reduce the resistance to the level where the display quality is not affected and reduce the power consumption using the divider resistor.

■ ELECTRICAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Supply voltage (1)	V_{SS}	-5 to +0.3	V
Supply voltage (2)	V_5	-7 to +0.3	V
Supply voltage (3)	V_1, V_4, V_2, V_3	V5 to +0.3	V
Input voltage	V_{IN}	Vss–0.3 to +0.3	V
Output voltage	V_O	Vss–0.3 to +0.3	V
Power dissipation	P_D	250	mW
Operating temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature time at lead	T_{sol}	260, 10	°C, sec

● **Absolute Maximum Ratings**

Notes: 1. All voltages are specified relative to V_{DD} = 0 V.
2. The following relation must be always hold
$V_{DD} > V_1 > V_2 > V_3 > V_4 > V_5$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

● **DC Characteristics**

(Ta = –40 to 85 °C, V_{DD} = 0 V unless stated otherwise)

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable Pin
Operating voltage (1) *1.	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V_5			–13.0	—	–3.5	V	V_5 *10.
	Allowable				–13.0	—	—		
	Allowable	V_1, V_2			0.6×V_5	—	V_{DD}	V	V_1, V_2
	Allowable	V_3, V_4			V_5	—	0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	*2, *3
		V_{IHC}			0.2×V_{SS}	—	V_{DD}		
		V_{IHT}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		*2, *3
		V_{IHC}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		
Low-level input voltage		V_{ILT}			V_{SS}		V_{SS}+0.8		*2, *3
		V_{ILC}			V_{SS}		0.8×V_{SS}		
		V_{ILT}	V_{SS} = –3 V		V_{SS}		0.85×V_{SS}		*2, *3
		V_{ILC}	V_{SS} = –3 V		V_{SS}		0.8×V_{SS}		
High-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		V_{SS}+2.4	—	—	V	OSC2 *4, *5
		V_{OHC1}	I_{OH} = –2.0 mA		V_{SS}+2.4	—	—		
		V_{OHC2}	I_{OH} = –120 µA		0.2×V_{SS}	—	—		
		V_{OHT}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}			V	*4, *5 OSC2
		V_{OHC1}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}				
		V_{OHC2}	V_{SS} = –3 V	I_{OH} = –50 µA	0.2×V_{SS}				

(continued)

● **DC Characteristics (Cont'd)**

(Ta = –40 to 80 °C, V_{DD} = 0 V unless stated otherwise)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable Pin
Low-level output voltage	V_{OLT}	I_{OL} = 3.0 mA		—	—	Vss+0.4	V	OSC2 *4, *5
	V_{OLC1}	I_{OL} = 2.0 mA		—	—	Vss+0.4		
	V_{OLC2}	I_{OL} = 120 µA		—	—	0.8×Vss		
	V_{OLT}	Vss = –3 V	I_{OL} = 2 mA			0.8×Vss	V	*4, *5 OSC2
	V_{OLC1}	Vss = –3 V	I_{OL} = 2 mA			0.8×Vss		
	V_{OLC2}	Vss = –3 V	I_{OL} = 50 µA			0.8×Vss		
Input leakage current	I_{LI}			–1.0	—	1.0	µA	*6
Output leakage current	I_{LO}			–3.0	—	3.0	µA	*7
LCD driver ON resistance	R_{ON}	Ta = 25 °C	V_5 = –5.0 V	—	5.0	7.5	kΩ	SEG0 to 79, COM0 to 15, *11
			V_5 = –3.5 V	—	10.0	50.0		
Static current dissipation	I_{DDQ}	$\overline{CS}$ = CL = V_{DD}		—	0.05	1.0	µA	V_{DD}
Dynamic current dissipation	I_{DD} (1)	During display V_5 = -7 V	f_{CL} = 2 kHz	—	2.0	5.0	µA	V_{DD} *12, *13, *14
			Rf = 1.5 MΩ	—	9.5	15.0		
			f_{CL} = 18 kHz	—	5.0	10.0		
		During display V_5 = -7 V Vss = -5 V	f_{CL} = 2 kHz		1.5	4.5	µA	V_{DD} *12, *13
			Rf = 1.5 MΩ		6.0	12.0		
	I_{DD} (2)	During access t_{cyc} = 200 kHz		—	300	500	µA	*8
		Vss = –3V, During access t_{cyc} = 200 kHz			150	300		
Input pin capacitance	C_{IN}	Ta = 25 deg. C, f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency	f_{OSC}	Rf = 1.5 MΩ ±2%, Vss = –5.0 V		15	18	21	kHz	*9
		Rf = 1.5 MΩ ±2%, Vss = –3.0 V		11	16	21		
Reset time	t_R			1.0	—		µS	$\overline{RES}$ *15

Notes: *1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.

*2. A0, D0 to D7, E (or $\overline{RD}$), R/W (or $\overline{WR}$) and $\overline{CS}$

*3. CL, FR, M/S and $\overline{RES}$

*4. D0 to D7

*5. FR

*6. A0, E (or $\overline{RD}$), R/W (or $\overline{WR}$), $\overline{CS}$, CL, M/S and $\overline{RES}$

*7. When D0 to D7 and FR are high impedance.

*8. During continual write access at a frequency of tcyc. Current consumption during access is effectively proportional to the access frequency.

*9. See figure below for details

*10. See figure below for details

*11. For a voltage differential of 0.1 V between input (V1, …, V4) and output (COM, SEG) pins. All voltages within specified operating voltage range.

*12. RW1020*A* and RW1021*A* and RW1022*A* only. Does not include transient currents due to stray and panel capacitances.

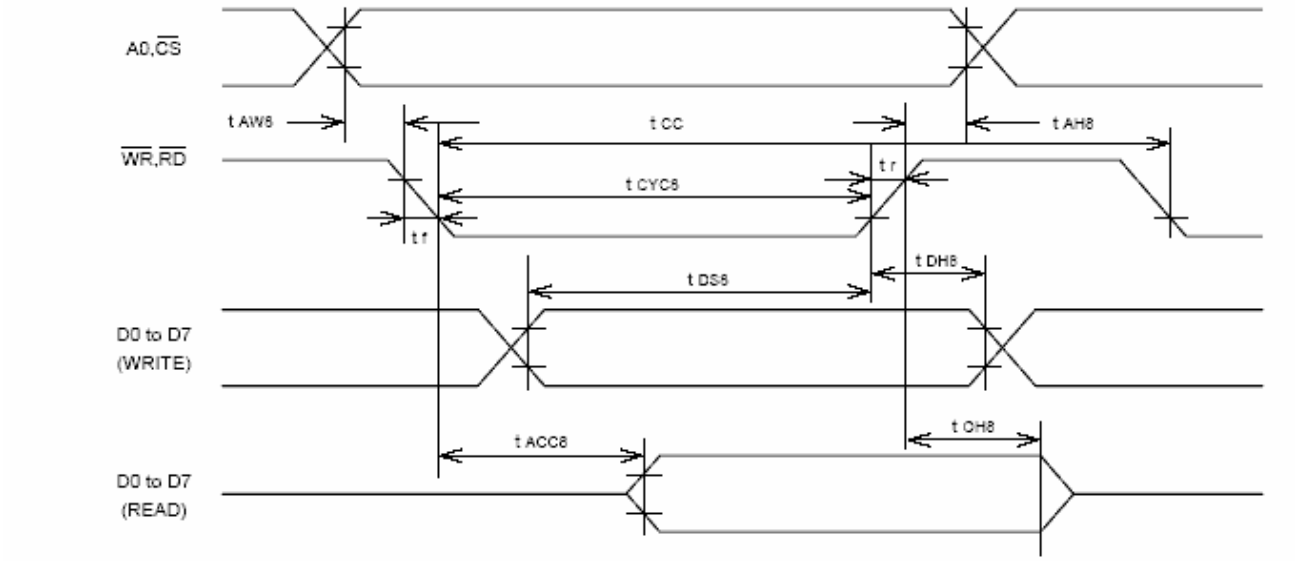
*13. RW1020*0* and RW1022*0* only. Does not include transient currents due to stray and panel capacitances.

*14. RW1021*0* only. Does not include transient currents due to stray and panel capacitances.

*15. tR (Reset time) represents the time from the $\overline{RES}$ signal edge to the completion of reset of the internal circuit. Therefore, the RW1020 series enters the normal operation status after this tR.

■ AC Characteristics

- MPU Bus Read/Write I (80-family MPU)



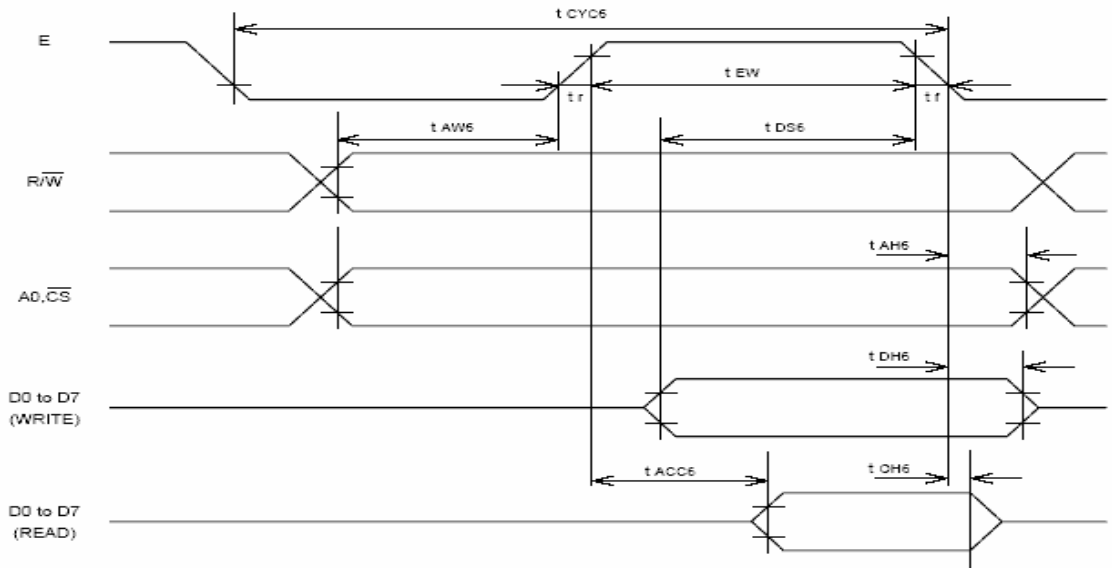
Ta=-20 to 75deg.C, Vss=-5.0V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min	Max		
Address hold time	tAH8		10	-	ns	A0, $\overline{CS}$
Address setup time	tAW8		20	-	ns	
System cycle time	tCYC8		1000	-	ns	$\overline{WR}$, $\overline{RD}$
Control pulsewidth	tCC		200	-	ns	
Data setup time	tDS8		80	-	ns	D0 to D7
Data hold time	tDH8		10	-	ns	
$\overline{RD}$ access time	tACC8	CL=100 pF	-	90	ns	
Output disable time	tCH8		10	60	ns	
Rise and fall time	tr,tf	-	-	15	ns	-

(Vss=-2.7V to -4.5V ,Ta=-20 to + 75℃)

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min	Max		
Address hold time	tAH8		20	-	ns	A0, $\overline{CS}$
Address setup time	tAW8		40	-	ns	
System cycle time	tCYC8		2000	-	ns	$\overline{WR}$, $\overline{RD}$
Control pulsewidth	tCC		400	-	ns	
Data setup time	tDS8		160	-	ns	D0 to D7
Data hold time	tDH8		20	-	ns	
$\overline{RD}$ access time	tACC8	CL=100 pF	-	180	ns	
Output disable time	tCH8		20	120	ns	
Rise and fall time	tr,tf	-	-	15	ns	-

- MPU Bus Read/Write II (68-family MPU)



Ta=-20 to 75deg.C, Vss=-5.0V ±10% unless stated otherwise

Parameter		Symbol	Condition	Rating		Unit	Signal
				Min	Max		
System cycle time		tCYC6		1000	-	ns	A0, $\overline{CS}$,R/W
Address setup time		tAW6		20	-	ns	
System cycle time		tAH6		10	-	ns	
Data setup time		tDS6		80	-	ns	D0 to D7
Data hold time		tDH6		10	-	ns	
Output disable time		tOH6	CL=100 pF	10	60	ns	
Access time		tACC6		-	90	ns	
Enable pulsewidth	Read	tEW		100	-	ns	E
	Write			80	-	ns	
Rise and fall time		tr,tf	-	-	15	ns	-

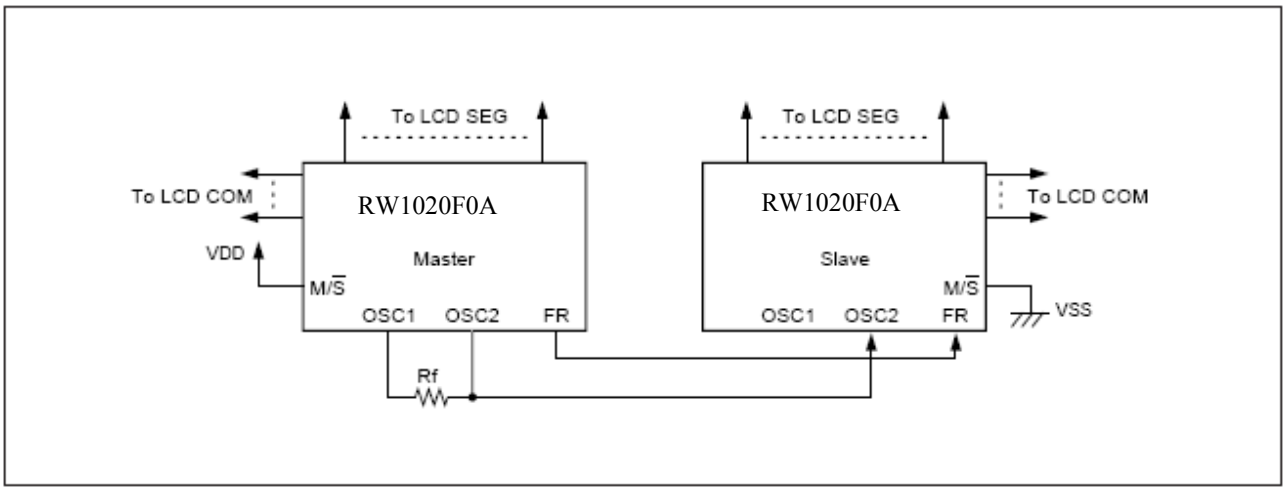
(Vss=-2.7V to -4.5V ,Ta=-20 to + 75℃)

Parameter		Symbol	Condition	Rating		Unit	Signal
				Min	Max		
System cycle time		tCYC6		2000	-	ns	A0, $\overline{CS}$,R/W
Address setup time		tAW6		40	-	ns	
System cycle time		tAH6		20	-	ns	
Data setup time		tDS6		160	-	ns	D0 to D7
Data hold time		tDH6		20	-	ns	
Output disable time		tOH6	CL=100 pF	20	120	ns	
Access time		tACC6		-	180	ns	
Enable pulsewidth	Read	tEW		200	-	ns	E
	Write			160	-	ns	
Rise and fall time		tr,tf	-	-	15	ns	-

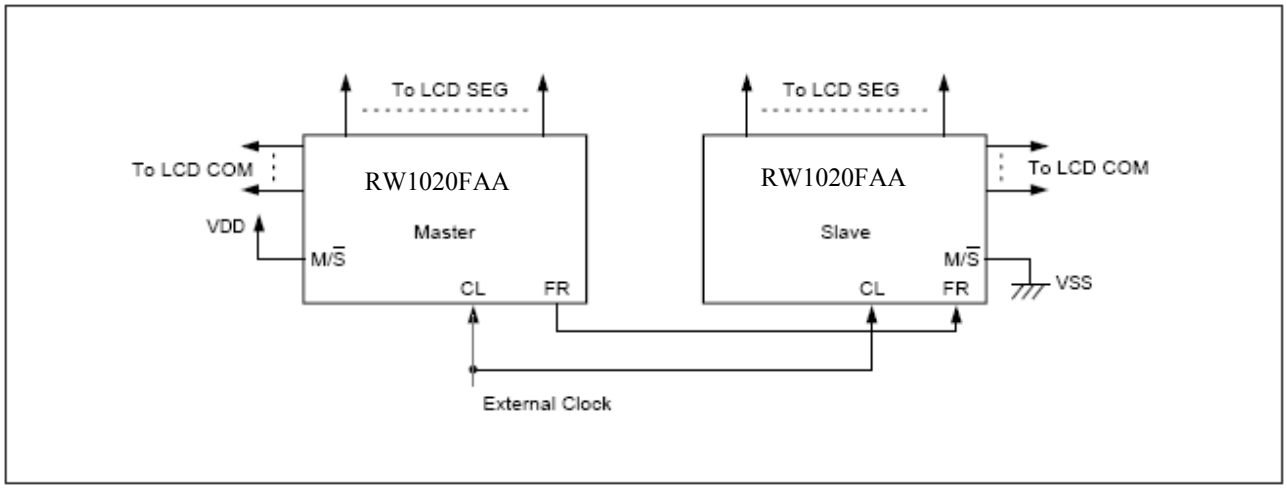
Note: 1.tCYC6 is the cycle time of $\overline{CS}$ .E=H, not the cycle time of E

■ LCD PANEL CONNECTION EXAMPLE

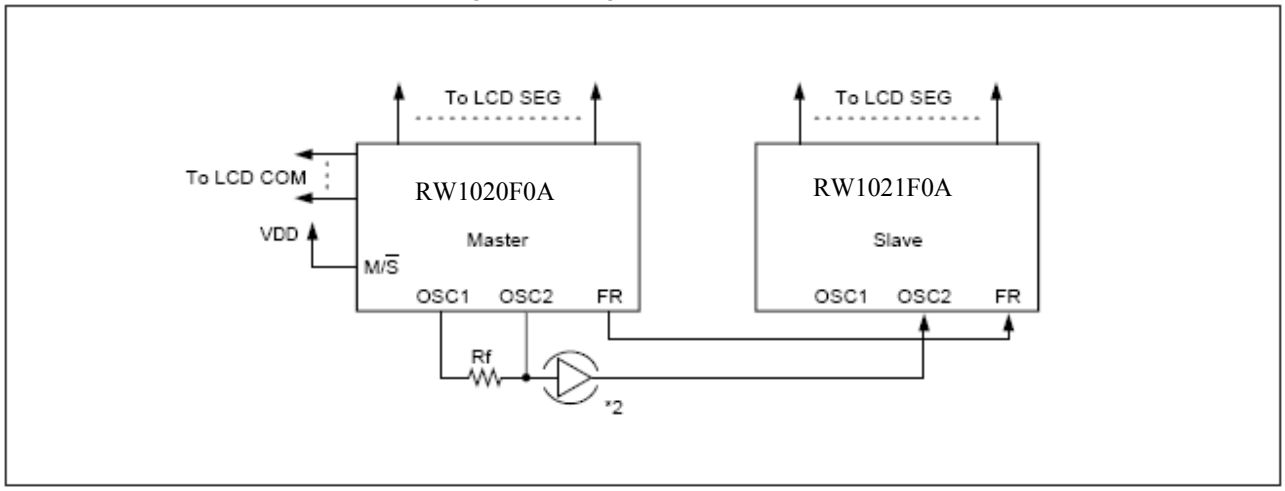
●RW1020F0A–RW1020F0A/RW1022F0A–RW1022F0A



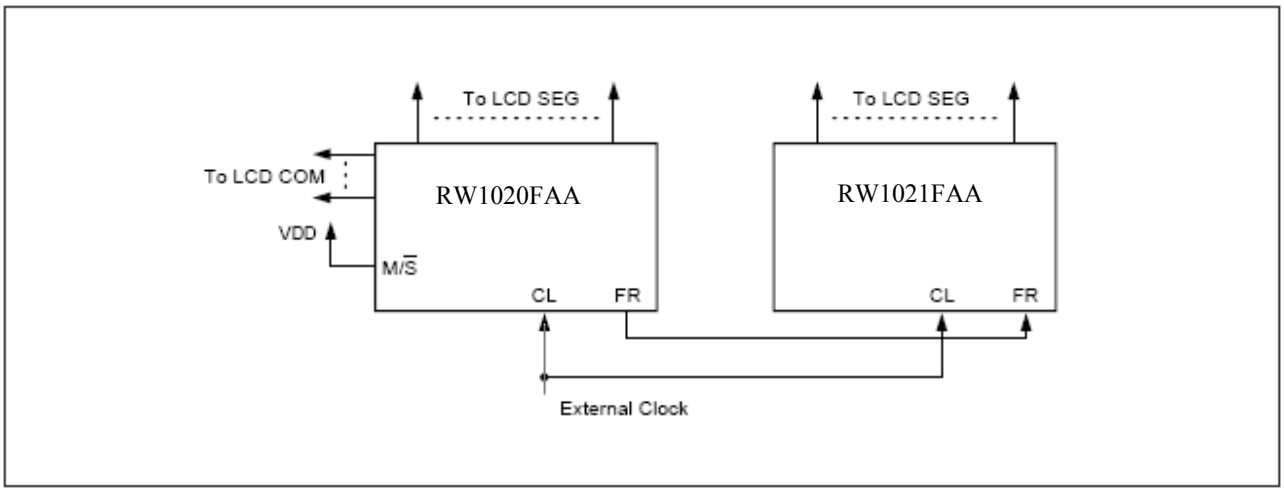
● RW1020FAA–RW1020FAA/RW1022FAA–RW1022FAA



●RW1020F0A/RW1022F0A–RW1021F0A (See note 1)



●**RW1020FAA–RW1021FAA**



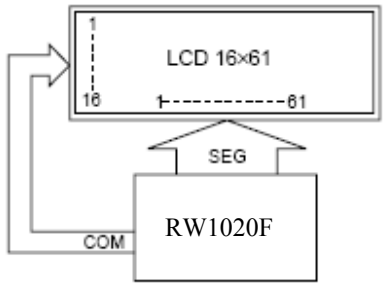
Notes: 1. the duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

■ LCD PANEL CONNECTION EXAMPLE

(The full-dot LCD panel displays a character in 6×8 dots.)

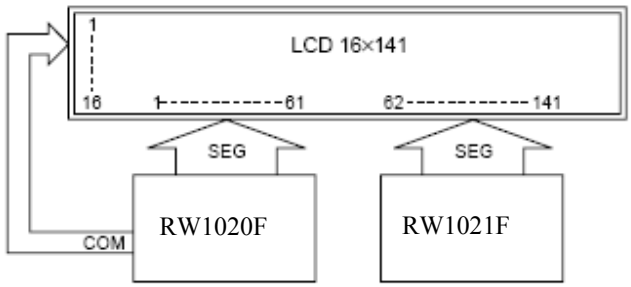
● 1/16 duty:

• 10 characters × 2 lines



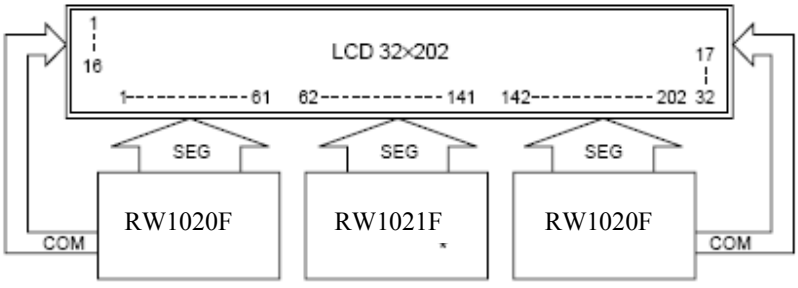
● 1/16 duty:

• 23 characters × 2 lines



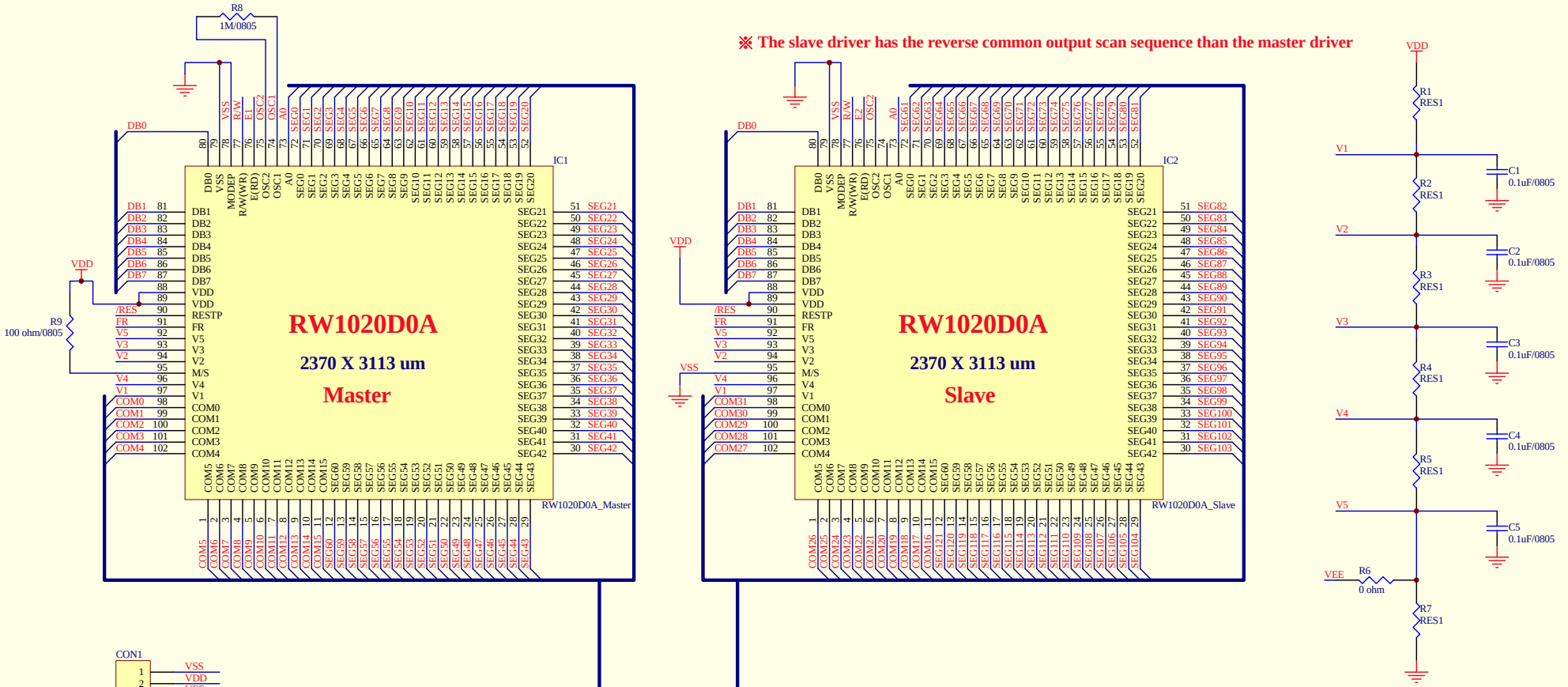
● 1/32 duty:

• 33 characters × 4 lines

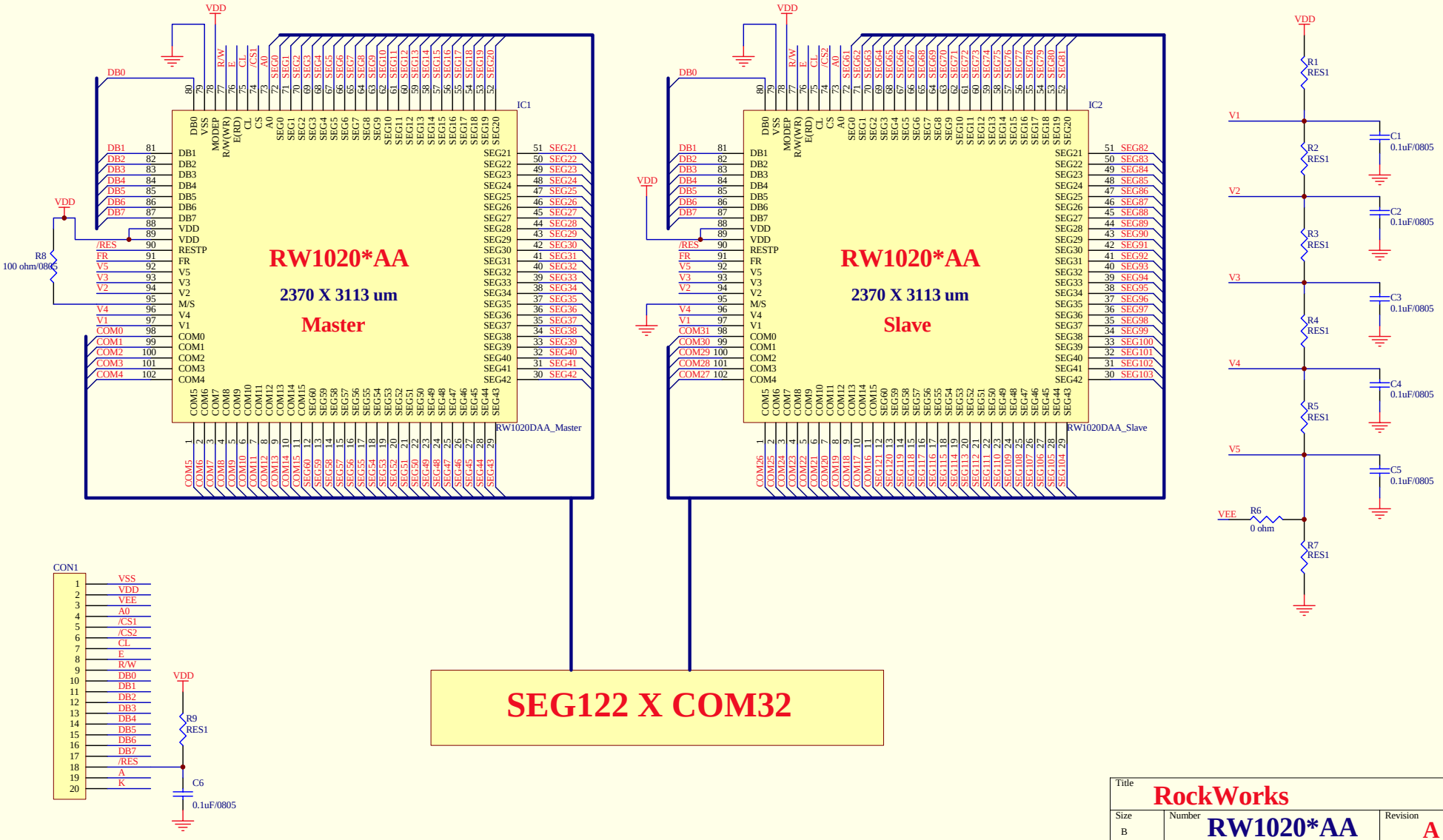


* The SED1521F can be omitted (the 32×122-dot display mode is selected).

Note: A combination of AB or AA type chip (that uses internal clocks) and 0B or 0A type chip (that uses external clocks) is NOT allowed.


※ The slave driver has the reverse common output scan sequence than the master driver
RW1020D0A
2370 X 3113 um
Master
RW1020D0A
2370 X 3113 um
Slave
SEG122 X COM32
RW1020D0A_Master
RW1020D0A_Slave
IC1
IC2
CON1
R8
1M/0805
R9
100 ohm/0805
R10
RES1
C6
0.1uF/0805
R1
RES1
R2
RES1
R3
RES1
R4
RES1
R5
RES1
R6
0 ohm
R7
RES1
C1
0.1uF/0805
C2
0.1uF/0805
C3
0.1uF/0805
C4
0.1uF/0805
C5
0.1uF/0805
VDD
VSS
VEE
V1
V2
V3
V4
V5
Title
RockWorks
Size
B
Number
RW1020*0A
Revision
A
Date:
21-Mar-2007
Sheet of
File:
C:\Documents and Settings\WillTai\桌面\99\RW1020*0A.ddb
Drawn By:

※ The slave driver has the reverse common output scan sequence than the master driver



SEG122 X COM32

Title	RockWorks	
Size: B	Number: RW1020*AA	Revision: A
Date: 21-Mar-2007	Sheet of	
File: C:\Documents and Settings\WillTai\桌面\99DaMyDesign.ddb		